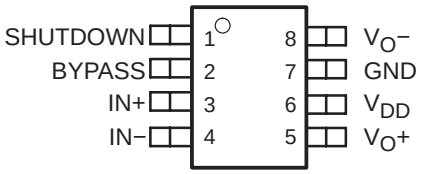
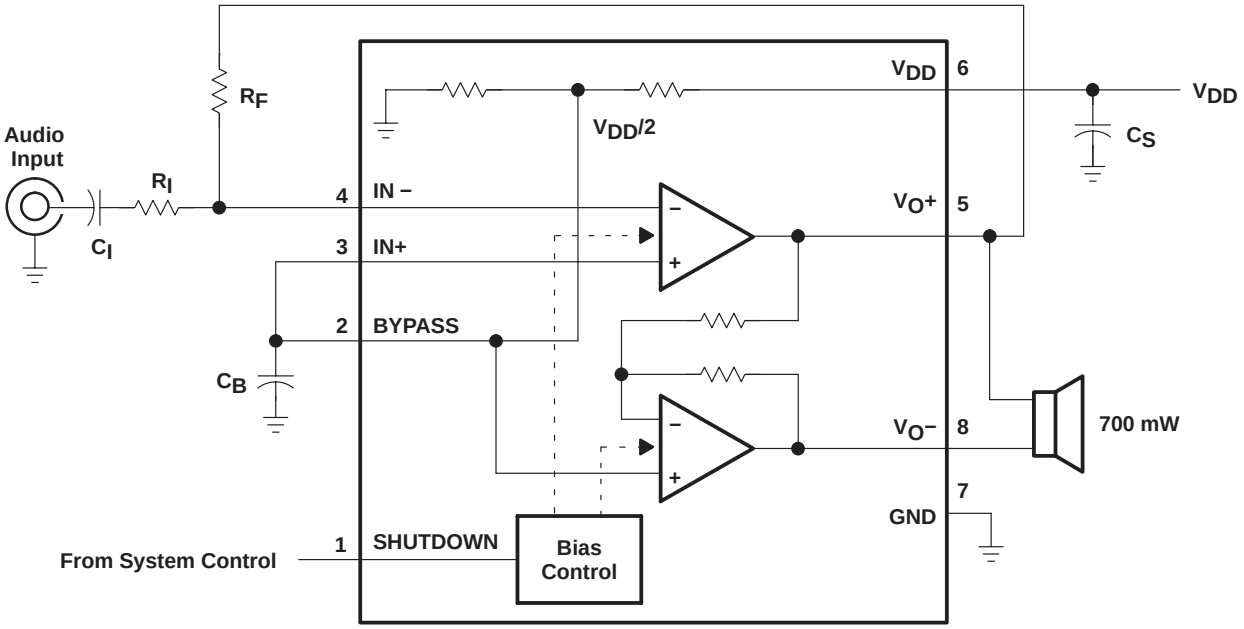
- **Fully Specified for 3.3-V and 5-V Operation**
- **Wide Power Supply Compatibility 2.5 V − 5.5 V**
- **Output Power for $R_L$ = 8 Ω**
  - **700 mW at $V_{DD}$ = 5 V**
  - **250 mW at $V_{DD}$ = 3.3 V**
- **Ultralow Supply Current in Shutdown Mode . . . 1.5 nA**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **SOIC**
  - **PowerPAD™ MSOP**

**D OR DGN PACKAGE (TOP VIEW)**




## description

The TPA731 is a bridge-tied load (BTL) audio power amplifier developed especially for low-voltage applications where internal speakers are required. Operating with a 3.3-V supply, the TPA731 can deliver 250-mW of continuous power into a BTL 8-Ω load at less than 0.6% THD+N throughout voice band frequencies. Although this device is characterized out to 20 kHz, its operation is optimized for narrower band applications such as wireless communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. This device features a shutdown mode for power-sensitive applications with a supply current of 1.5 nA during shutdown. The TPA731 is available in an 8-pin SOIC surface-mount package and the surface-mount PowerPAD™ MSOP, which reduces board space by 50% and height by 40%.




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**AVAILABLE OPTIONS**

| $T_A$ | PACKAGED DEVICES | | MSOP SYMBOLIZATION |
|---|---|---|---|
| | SMALL OUTLINE† (D) | MSOP‡ (DGN) | |
| −40°C to 85°C | TPA731D | TPA731DGN | AJC |

† In the SOIC package, the maximum RMS output power is thermally limited to 350 mW; 700 mW peaks can be driven, as long as the RMS value is less than 350 mW.
‡ The D and DGN packages are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA731DR).

## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| BYPASS | 2 | I | BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-µF to 2.2-µF capacitor when used as an audio amplifier. |
| GND | 7 | | GND is the ground connection. |
| IN− | 4 | I | IN− is the inverting input. IN− is typically used as the audio input terminal. |
| IN+ | 3 | I | IN+ is the noninverting input. IN+ is typically tied to the BYPASS terminal for SE operations. |
| SHUTDOWN | 1 | I | SHUTDOWN places the entire device in shutdown mode when held high ($I_{DD}$ = 1.5 nA). |
| $V_{DD}$ | 6 | | $V_{DD}$ is the supply voltage terminal. |
| $V_O$+ | 5 | O | $V_O$+ is the positive BTL output. |
| $V_O$− | 8 | O | $V_O$− is the negative BTL output. |

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, $V_{DD}$ . . . . . 6 V
Input voltage, $V_I$ . . . . . −0.3 V to $V_{DD}$ +0.3 V
Continuous total power dissipation . . . . . Internally limited (see Dissipation Rating Table)
Operating free-air temperature range, $T_A$ . . . . . −40°C to 85°C
Operating junction temperature range, $T_J$ . . . . . −40°C to 150°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ | DERATING FACTOR | $T_A$ = 70°C | $T_A$ = 85°C |
|---|---|---|---|---|
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW |
| DGN | 2.14 W¶ | 17.1 mW/°C | 1.37 W | 1.11 W |

¶ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of that document.

## recommended operating conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{DD}$ | 2.5 | 5.5 | V |
| High-level voltage, $V_{IH}$ (SHUTDOWN) | $0.9V_{DD}$ | | V |
| Low-level voltage, $V_{IL}$ (SHUTDOWN) | | $0.1V_{DD}$ | V |
| Operating free-air temperature, $T_A$ | −40 | 85 | °C |

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 3.3 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\|V_{OS}\|$ | Output offset voltage (measured differentially) | SHUTDOWN = 0 V, $R_L$ = 8 Ω, RF = 10 kΩ | | | 20 | mV |
| PSRR | Power supply rejection ratio | $V_{DD}$ = 3.2 V to 3.4 V | | 85 | | dB |
| $I_{DD}$ | Supply current | SHUTDOWN = 0 V, RF = 10 kΩ | | 1.25 | 2.5 | mA |
| $I_{DD(SD)}$ | Supply current, shutdown mode (see Figure 4) | SHUTDOWN = $V_{DD}$, RF = 10 kΩ | | 1.5 | 1000 | nA |
| $\|I_{IH}\|$ | | SHUTDOWN, $V_{DD}$ = 3.3 V, $V_i$ = 3.3 V | | | 1 | µA |
| $\|I_{IL}\|$ | | SHUTDOWN, $V_{DD}$ = 3.3 V, $V_i$ = 0 V | | | 1 | µA |

## operating characteristics, $V_{DD}$ = 3.3 V, $T_A$ = 25°C, $R_L$ = 8 Ω

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $P_O$ | Output power, See Note 1 | THD = 0.2%, | See Figure 9 | | | 250 | | mW |
| THD + N | Total harmonic distortion plus noise | $P_O$ = 250 mW, | f = 200 Hz to 4 kHz, | See Figure 7 | | 0.55% | | |
| $B_{OM}$ | Maximum output power bandwidth | $A_V$ = −2 V/V, | THD = 2%, | See Figure 7 | | 20 | | kHz |
| $B_1$ | Unity-gain bandwidth | Open Loop, | See Figure 15 | | | 1.4 | | MHz |
| | Supply ripple rejection ratio | f = 1 kHz, | $C_B$ = 1 µF, | See Figure 2 | | 79 | | dB |
| $V_n$ | Noise output voltage | $A_V$ = −1V/V, | $C_B$ = 0.1 µF, | See Figure 19 | | 17 | | µV(rms) |

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 5 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\|V_{OS}\|$ | Output offset voltage (measured differentially) | SHUTDOWN = 0 V, $R_L$ = 8 Ω, RF = 10 kΩ | | | 20 | mV |
| PSRR | Power supply rejection ratio | $V_{DD}$ = 4.9 V to 5.1 V | | 78 | | dB |
| $I_{DD}$ | Supply current | SHUTDOWN = 0 V, RF = 10 kΩ | | 1.55 | 2.5 | mA |
| $I_{DD(SD)}$ | Supply current, shutdown mode (see Figure 4) | SHUTDOWN = $V_{DD}$ RF = 10 kΩ | | 5 | 1500 | nA |
| $\|I_{IH}\|$ | | SHUTDOWN, $V_{DD}$ = 5.5 V, $V_i$ = $V_{DD}$ | | | 1 | µA |
| $\|I_{IL}\|$ | | SHUTDOWN, $V_{DD}$ = 5.5 V, $V_i$ = 0 V | | | 1 | µA |

## operating characteristics, $V_{DD}$ = 5 V, $T_A$ = 25°C, $R_L$ = 8 Ω

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $P_O$ | Output power | THD = 0.5%, | See Figure 13 | | | 700† | | mW |
| THD + N | Total harmonic distortion plus noise | $P_O$ = 250 mW, | f = 200 Hz to 4 kHz, | See Figure 11 | | 0.5% | | |
| $B_{OM}$ | Maximum output power bandwidth | $A_V$ = −2 V/V, | THD = 2%, | See Figure 11 | | 20 | | kHz |
| $B_1$ | Unity-gain bandwidth | Open Loop, | See Figure 16 | | | 1.4 | | MHz |
| | Supply ripple rejection ratio | f = 1 kHz, | $C_B$ = 1 µF, | See Figure 2 | | 80 | | dB |
| $V_n$ | Noise output voltage | $A_V$ = −1 V/V, | $C_B$ = 0.1 µF, | See Figure 20 | | 17 | | µV(rms) |

† The DGN package, properly mounted, can conduct 700 mW RMS power continuously. The D package, can only conduct 350 mW RMS power continuously, with peaks to 700 mW.

## PARAMETER MEASUREMENT INFORMATION

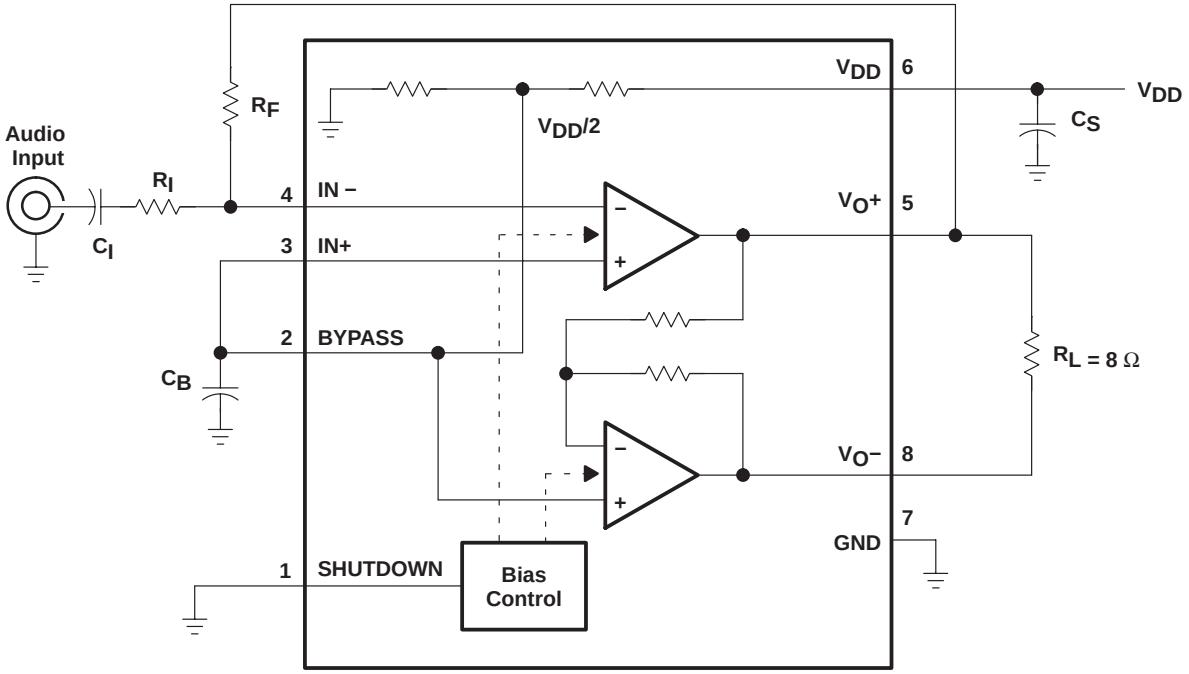



**Figure 1. BTL Mode Test Circuit**

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $k_{SVR}$ | Supply ripple rejection ratio | vs Frequency | 2 |
| $I_{DD}$ | Supply current | vs Supply voltage | 3, 4 |
| $P_O$ | Output power | vs Supply voltage | 5 |
| | | vs Load resistance | 6 |
| THD + N | Total harmonic distortion plus noise | vs Frequency | 7, 8, 11, 12 |
| | | vs Output power | 9, 10, 13, 14 |
| | Open loop gain and phase | vs Frequency | 15, 16 |
| | Closed loop gain and phase | vs Frequency | 17, 18 |
| $V_n$ | Output noise voltage | vs Frequency | 19, 20 |
| $P_D$ | Power dissipation | vs Output power | 21, 22 |

## TYPICAL CHARACTERISTICS

**SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY**

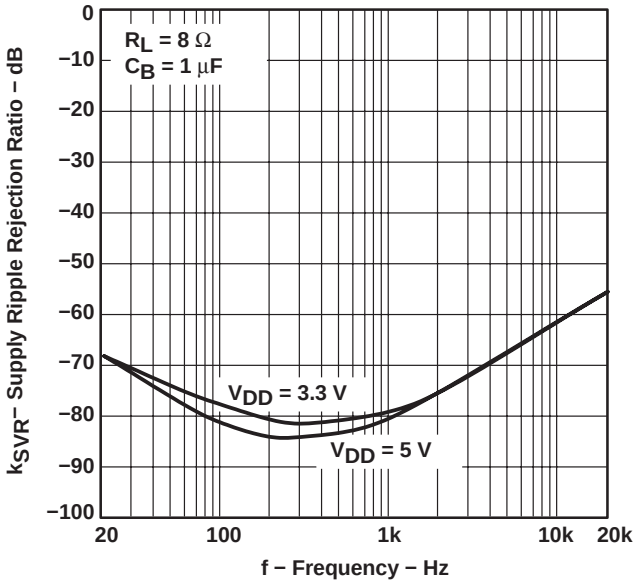



**Figure 2**

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

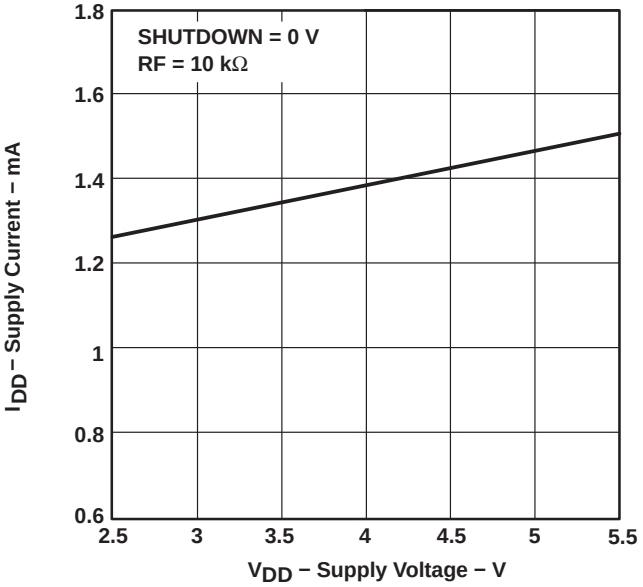



**Figure 3**

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

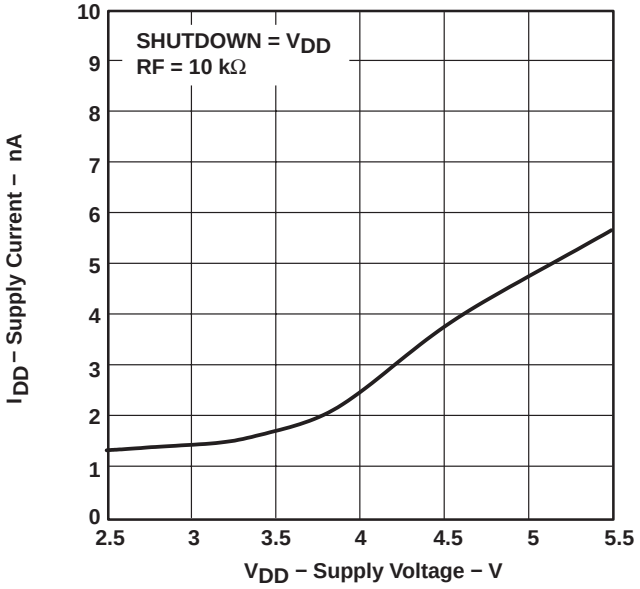



**Figure 4**

## TYPICAL CHARACTERISTICS

**OUTPUT POWER**
**vs**
**SUPPLY VOLTAGE**

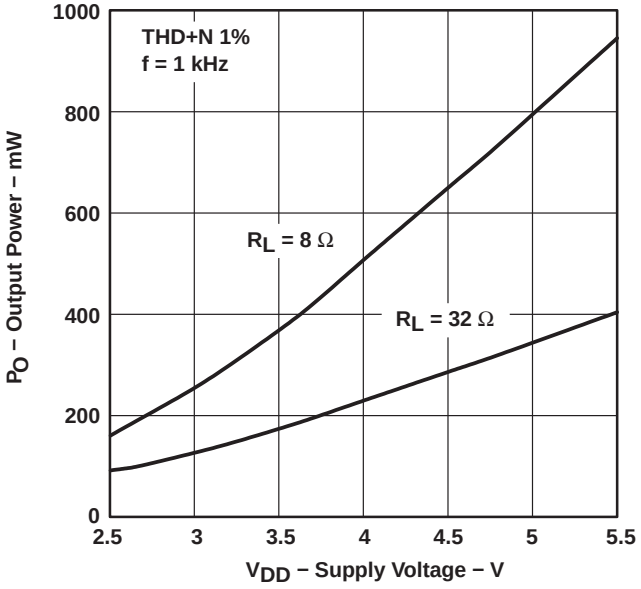



**Figure 5**

**OUTPUT POWER**
**vs**
**LOAD RESISTANCE**

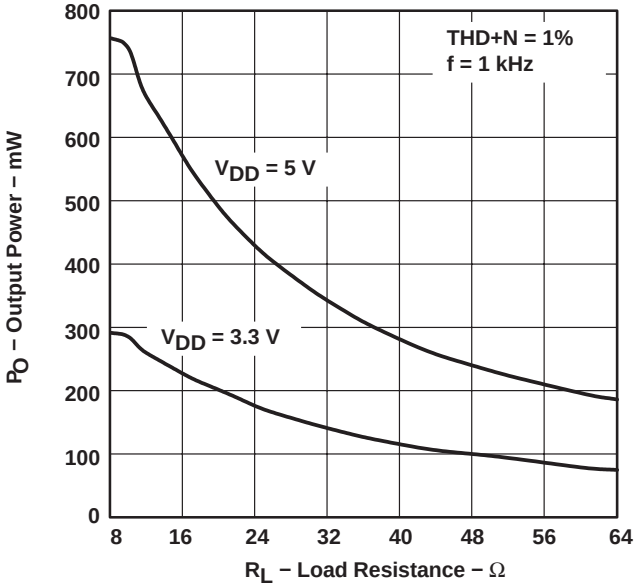



**Figure 6**

## TYPICAL CHARACTERISTICS

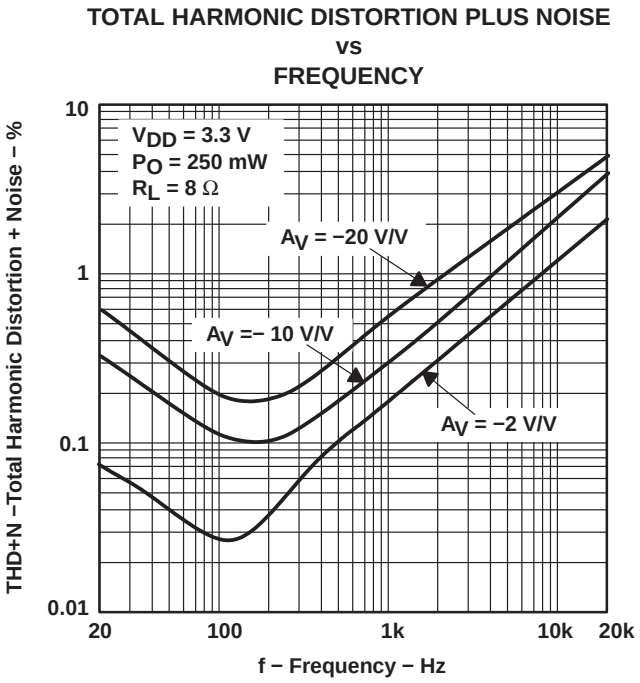



Figure 7

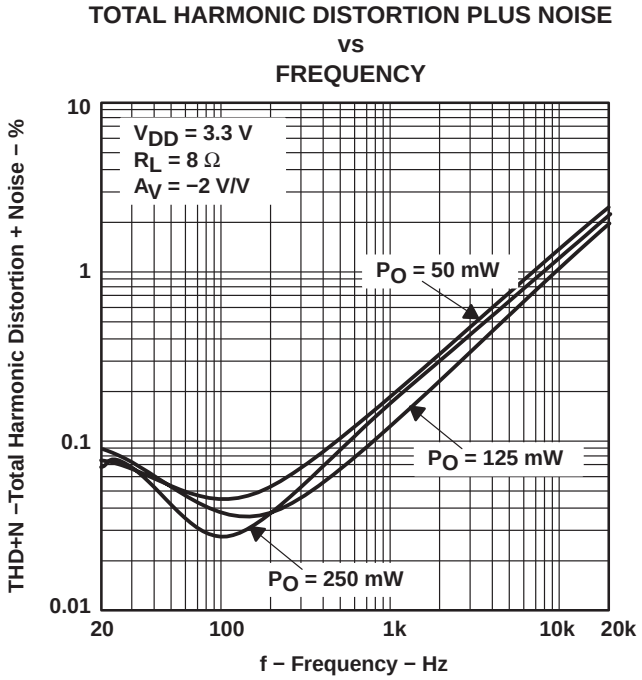



Figure 8

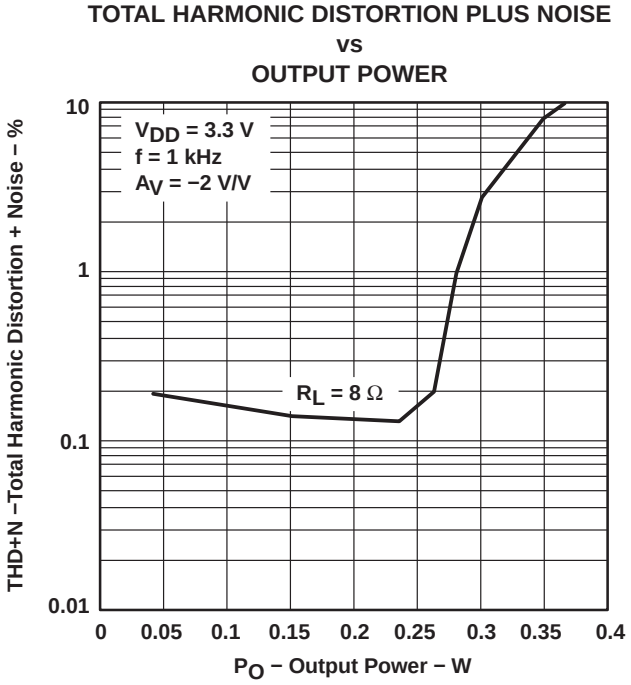



Figure 9

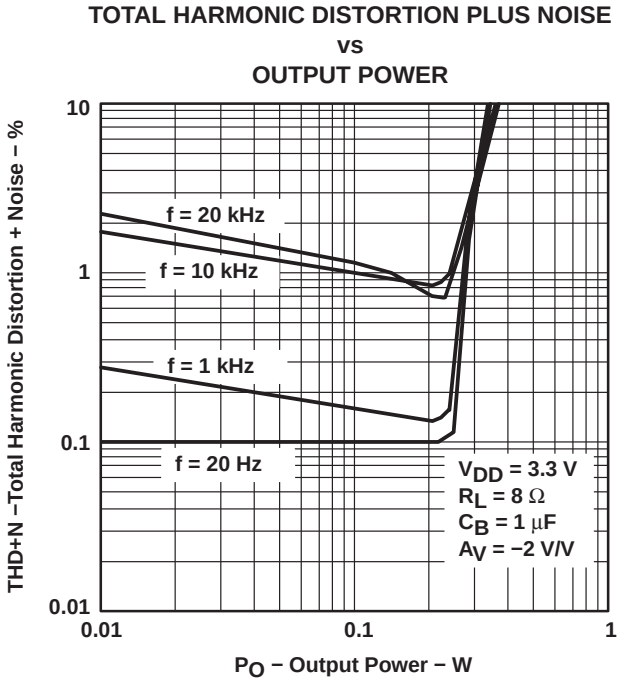



Figure 10

## TYPICAL CHARACTERISTICS

**TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY**

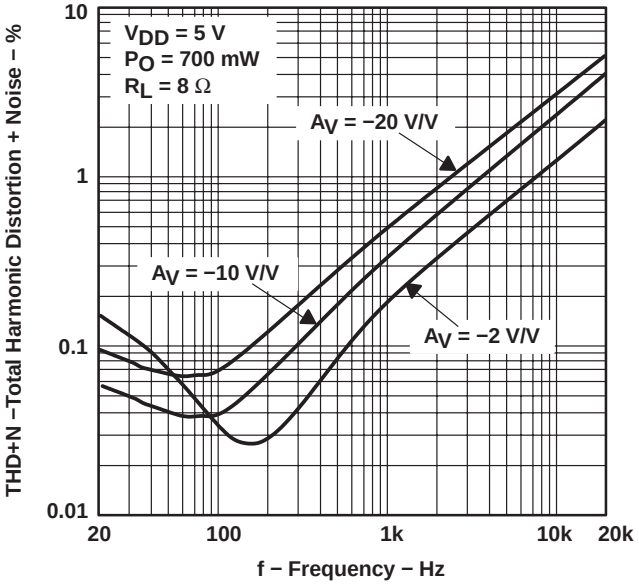



**Figure 11**

**TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY**

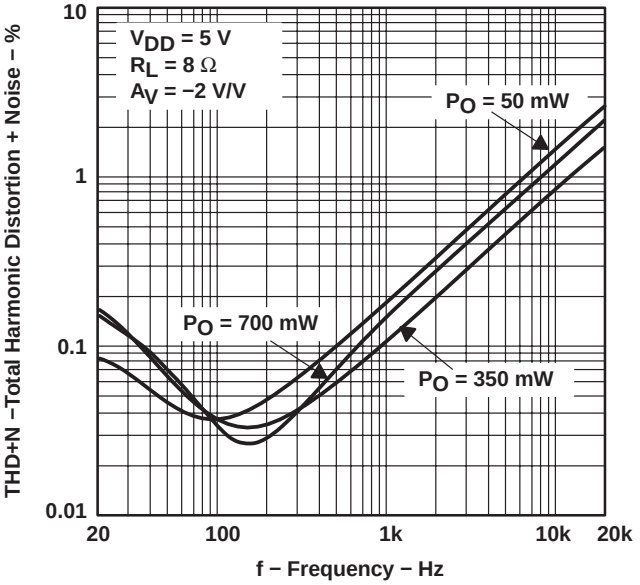



**Figure 12**

**TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER**

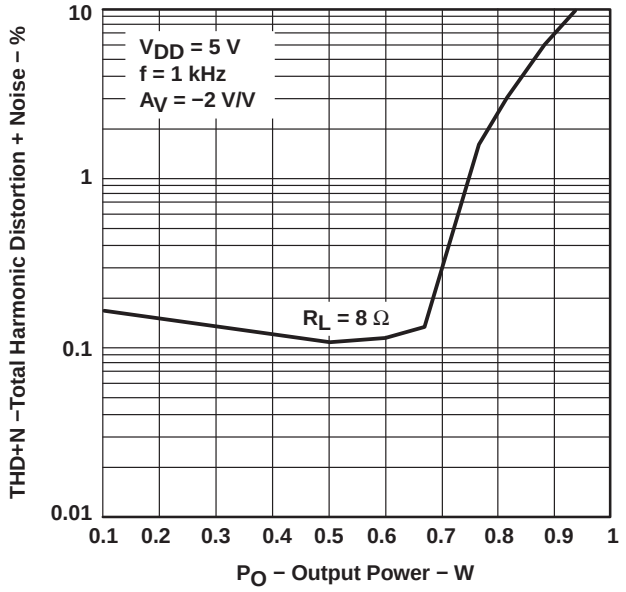



**Figure 13**

**TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER**

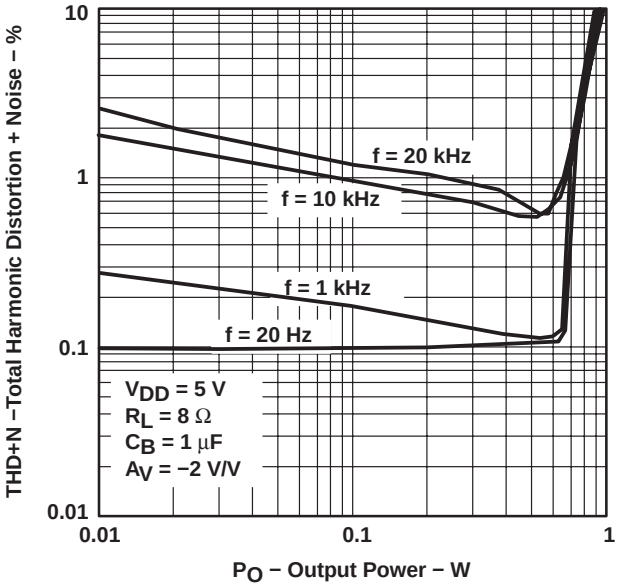



**Figure 14**

## TYPICAL CHARACTERISTICS

**OPEN-LOOP GAIN AND PHASE vs FREQUENCY**

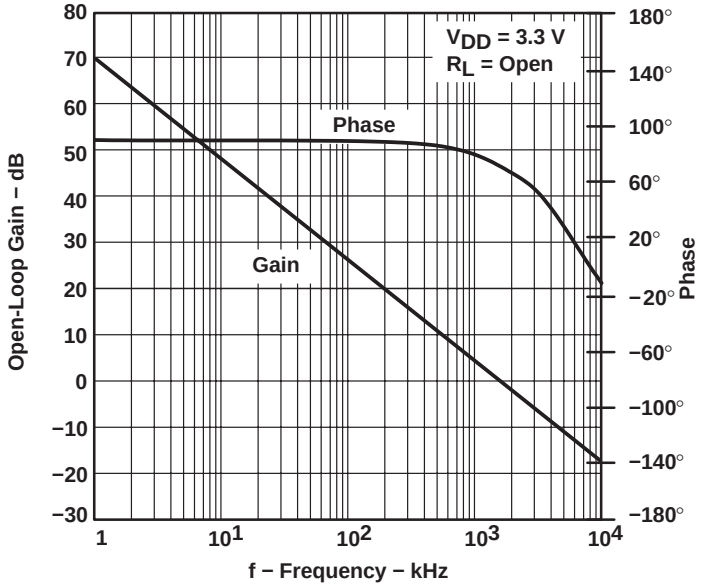



**Figure 15**

**OPEN-LOOP GAIN AND PHASE vs FREQUENCY**

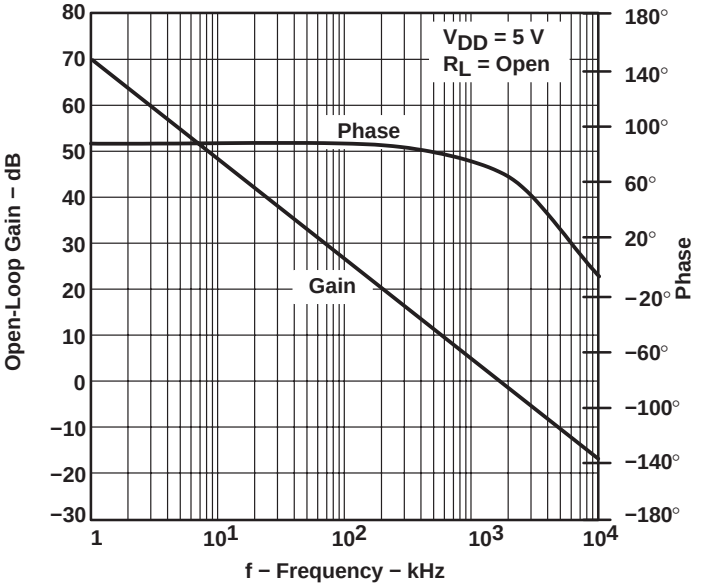



**Figure 16**

## TYPICAL CHARACTERISTICS

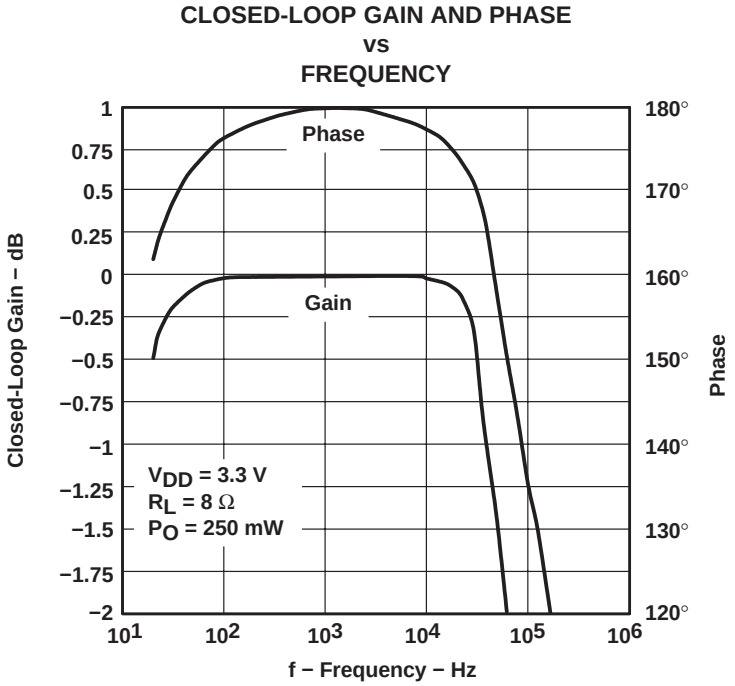



**Figure 17**

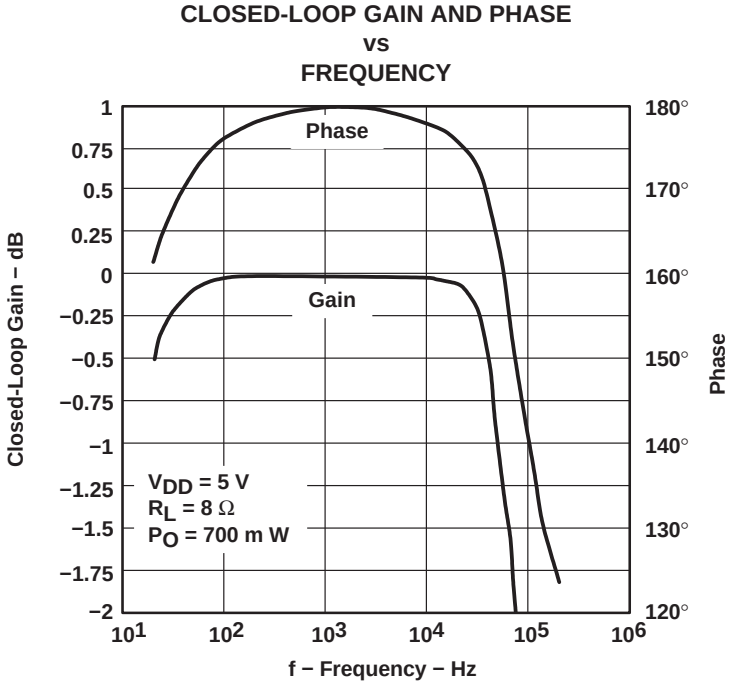



**Figure 18**

## TYPICAL CHARACTERISTICS

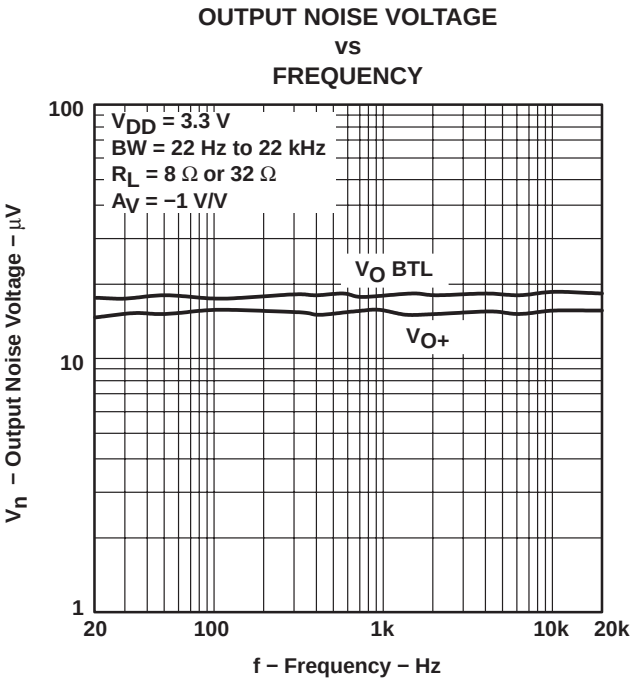



Figure 19

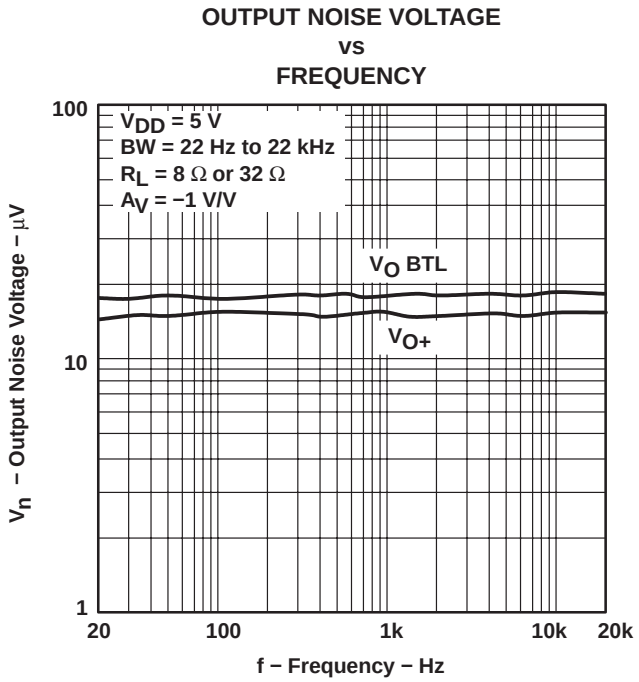



Figure 20

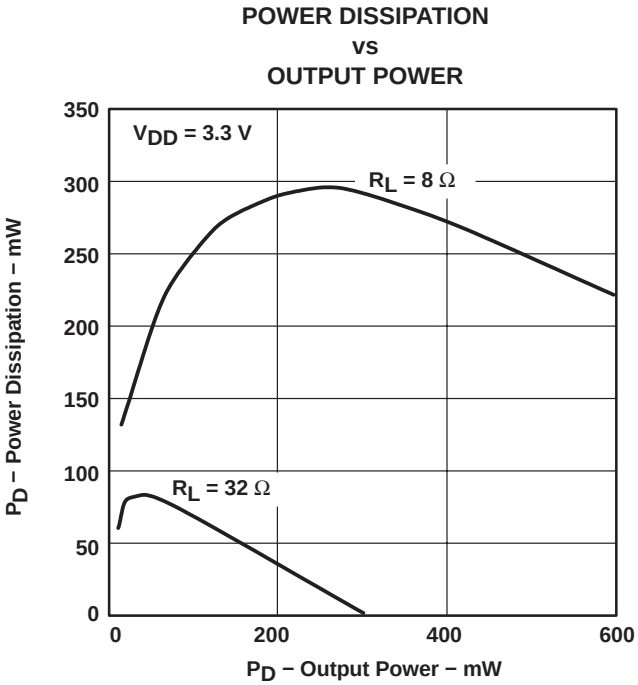



Figure 21

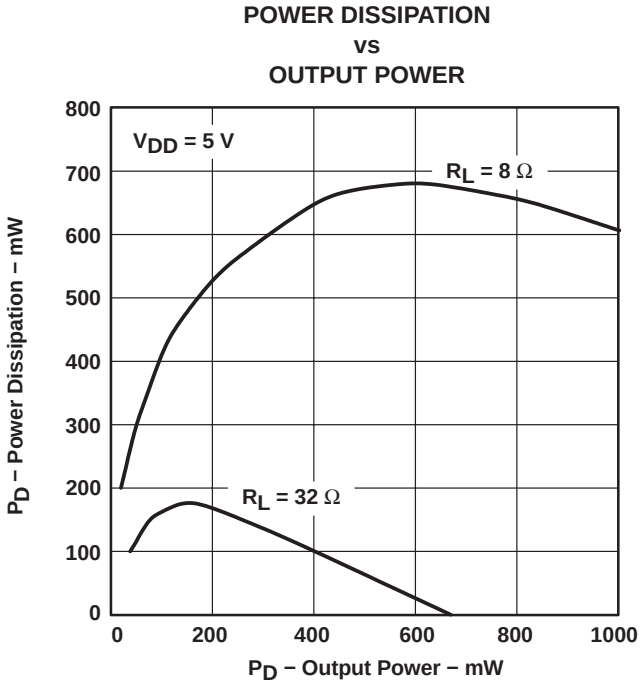



Figure 22

## APPLICATION INFORMATION

### bridged-tied load

Figure 23 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA731 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This, in effect, doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^{2}}{R_L} \qquad (1)$$

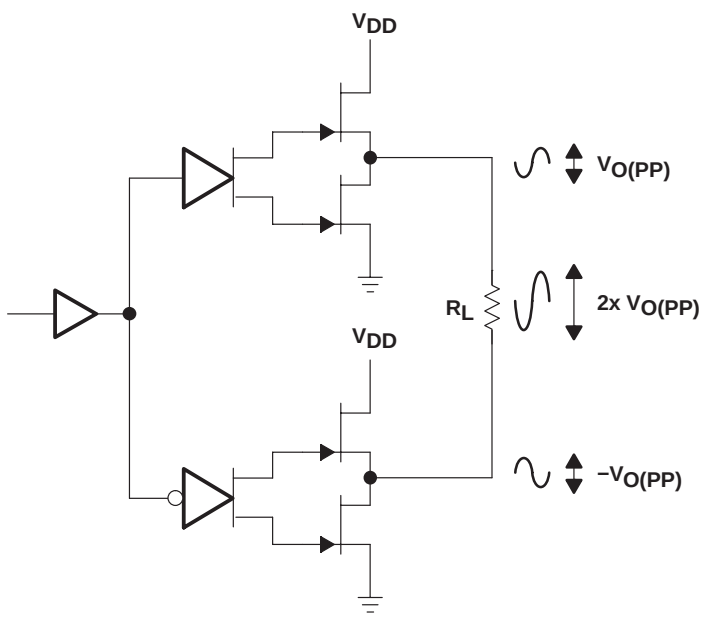



**Figure 23. Bridge-Tied Load Configuration**

In a typical portable handheld equipment sound channel operating at 3.3 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 62.5 mW to 250 mW. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power, there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 24. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency-limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_c = \frac{1}{2\pi R_L C_C} \qquad (2)$$

## APPLICATION INFORMATION

### bridged-tied load (continued)

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

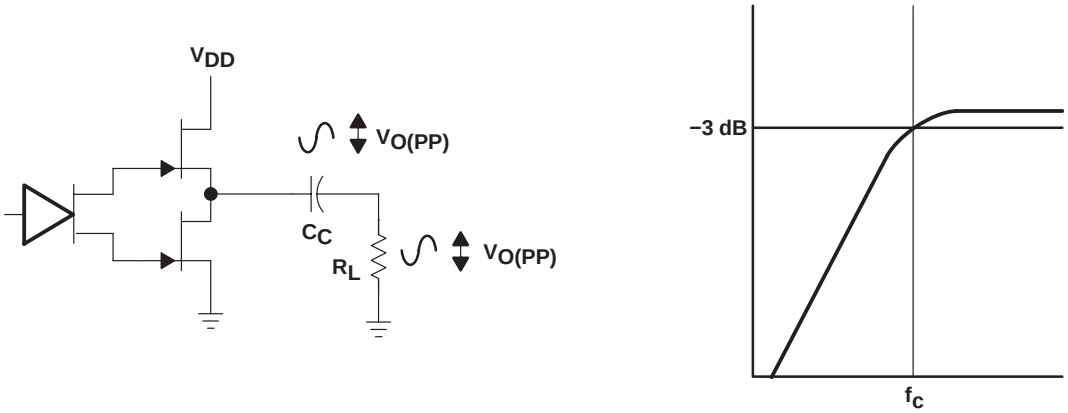



**Figure 24. Single-Ended Configuration and Frequency Response**

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of a SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

### BTL amplifier efficiency

The primary cause of linear amplifiers inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from $V_{DD}$. The internal voltage drop multiplied by the RMS value of the supply current, $I_{DD}$rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 25).

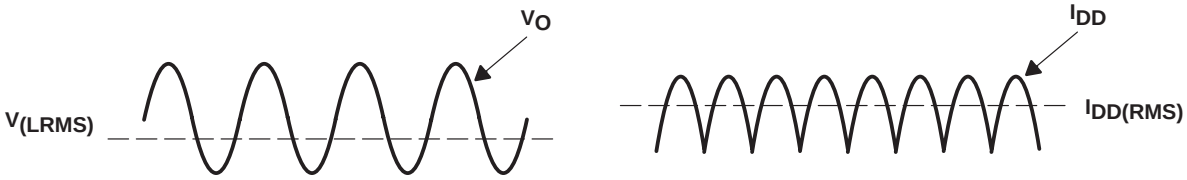



**Figure 25. Voltage and Current Waveforms for BTL Amplifiers**

## APPLICATION INFORMATION

### BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

where

$$P_L = \frac{V_L rms^2}{R_L} = \frac{V_p^2}{2R_L}$$

$$V_L rms = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\, I_{DD} rms = \frac{V_{DD}\, 2V_P}{\pi R_L}$$

$$I_{DD} rms = \frac{2V_P}{\pi R_L}$$

$$\text{Efficiency of a BTL configuration} = \frac{\pi V_P}{4V_{DD}} = \frac{\pi \left(2 P_L R_L\right)^{1/2}}{4V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for three different output power levels. The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased, resulting in a nearly flat internal power dissipation over the normal operating range. The internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design.

**Table 1. Efficiency vs Output Power in 3.3-V 8-Ω BTL Systems**

| OUTPUT POWER (W) | EFFICIENCY (%) | PEAK VOLTAGE (V) | INTERNAL DISSIPATION (W) |
|---|---|---|---|
| 0.125 | 33.6 | 1.41 | 0.26 |
| 0.25 | 47.6 | 2.00 | 0.29 |
| 0.375 | 58.3 | 2.45† | 0.28 |

† High-peak voltage values cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. In equation 4, $V_{DD}$ is in the denominator. This indicates that as $V_{DD}$ goes down, efficiency goes up.

## APPLICATION INFORMATION

### application schematics

Figure 26 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of −10 V/V.

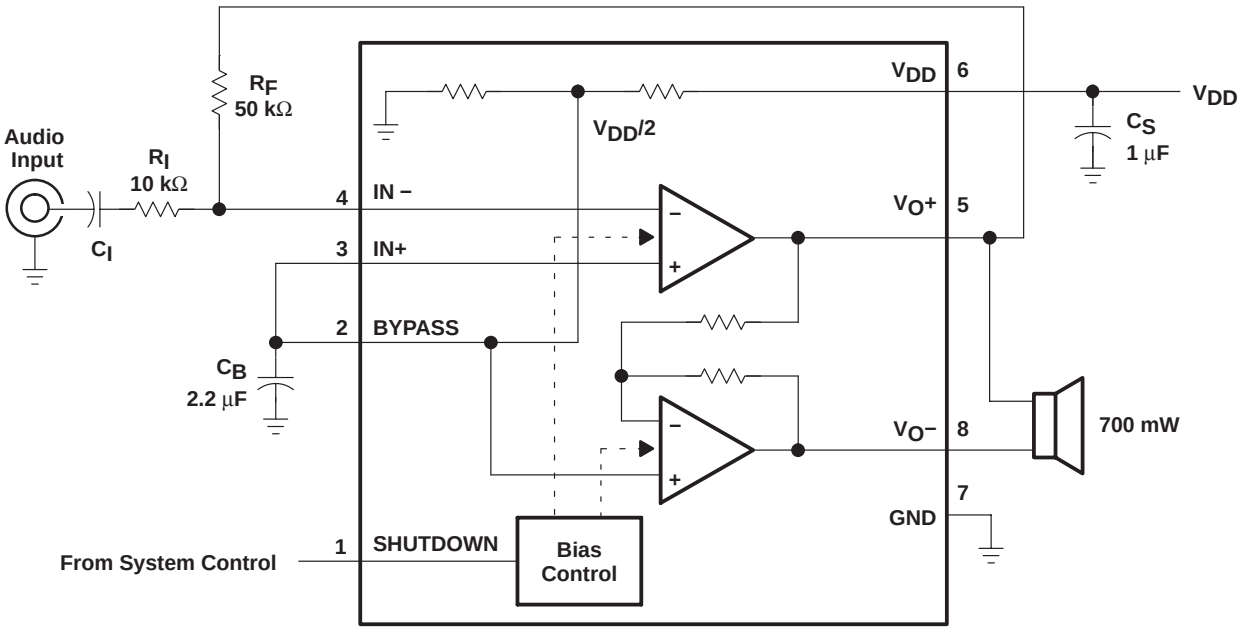



**Figure 26. TPA731 Application Circuit**

Figure 27 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of −10 V/V with a differential input.

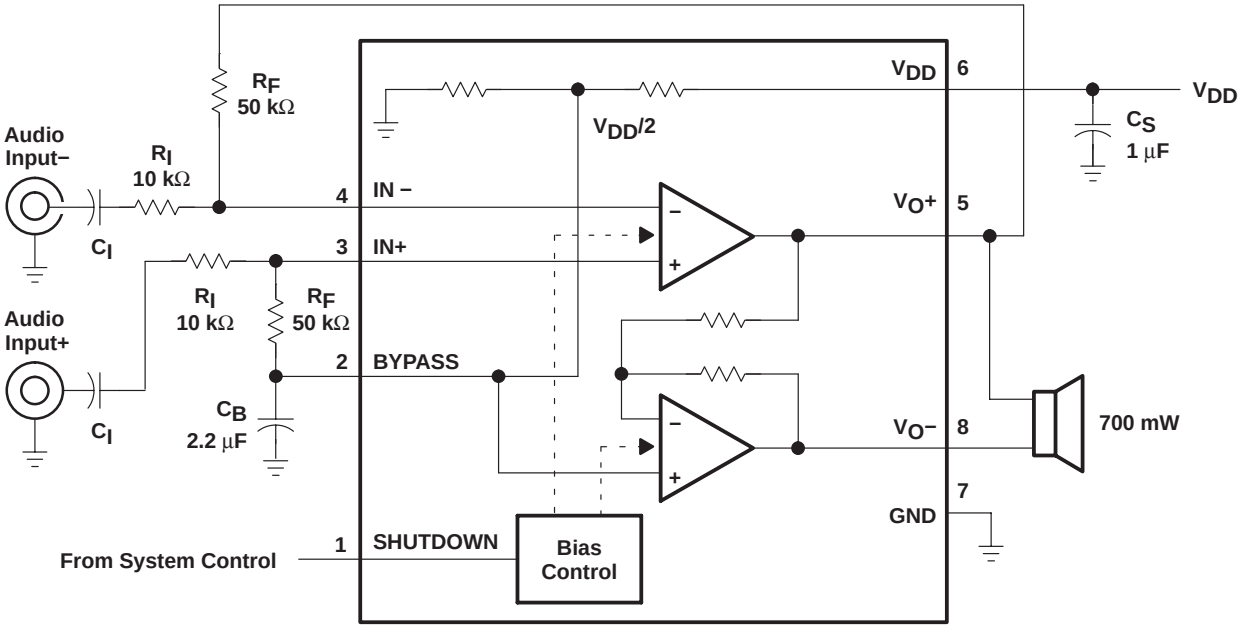



**Figure 27. TPA731 Application Circuit With Differential Input**

## APPLICATION INFORMATION

### application schematics (continued)

It is important to note that using the additional $R_F$ resistor connected between IN+ and BYPASS causes $V_{DD}/2$ to shift slightly, which could influence the THD+N performance of the amplifier. Although an additional external op-amp could be used to buffer BYPASS from $R_F$, tests in the lab have shown that the THD+N performance is only minimally affected by operating in the fully differential mode as shown in Figure 27. The following sections discuss the selection of the components used in Figures 26 and 27.

### component selection

#### gain setting resistors, $R_F$ and $R_I$

The gain for each audio input of the TPA731 is set by resistors $R_F$ and $R_I$ according to equation 5 for BTL mode.

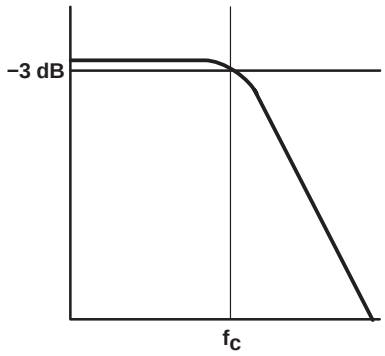
$$\text{BTL gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA731 is a MOS amplifier, the input impedance is very high; consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of $R_F$ increases. In addition, a certain range of $R_F$ values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\text{Effective impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be −10 V/V and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of $R_F$ above 50 kΩ, the amplifier tends to become unstable due to a pole formed from $R_F$ and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with $R_F$ when $R_F$ is greater than 50 kΩ. This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 7.



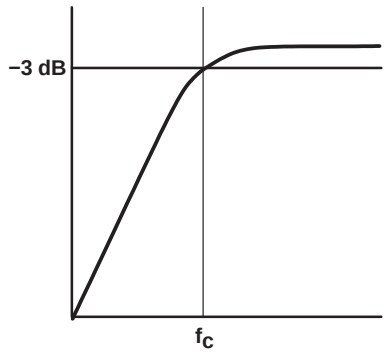

$$f_c = \frac{1}{2\pi R_F C_F} \tag{7}$$

For example, if $R_F$ is 100 kΩ and $C_F$ is 5 pF, then $f_c$ is 318 kHz, which is well outside of the audio range.

## APPLICATION INFORMATION

### input capacitor, $C_I$

In the typical application an input capacitor, $C_I$, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, $C_I$ and $R_I$ form a high-pass filter with the corner frequency determined in equation 8.




$$f_c = \frac{1}{2\pi R_I C_I} \tag{8}$$

The value of $C_I$ is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where $R_I$ is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_c} \tag{9}$$

In this example, $C_I$ is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network ($R_I$, $C_I$) and the feedback resistor ($R_F$) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

### power supply decoupling, $C_S$

The TPA731 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device $V_{DD}$ lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

## APPLICATION INFORMATION

### midrail bypass capacitor, $C_B$

The midrail bypass capacitor, $C_B$, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, $C_B$ determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD + N. The capacitor is fed from a 250-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained. This insures the input capacitor is fully charged before the bypass capacitor is fully charged and the amplifier starts up.

$$\frac{10}{\left(C_B \times 250\ k\Omega\right)} \leq \frac{1}{\left(R_F + R_I\right) C_I} \tag{10}$$

As an example, consider a circuit where $C_B$ is 2.2 µF, $C_I$ is 0.47 µF, $R_F$ is 50 kΩ, and $R_I$ is 10 kΩ. Inserting these values into the equation 10 we get:

$$18.2 \leq 35.5$$

which satisfies the rule. Bypass capacitor, $C_B$, values of 0.1 µF to 2.2 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

### using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

### 5-V versus 3.3-V operation

The TPA731 operates over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation with respect to supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in TPA731 can produce a maximum voltage swing of $V_{DD}$ − 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to $V_{O(PP)}$ = 4 V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power of operation from 5-V supplies for a given output-power level.

## APPLICATION INFORMATION

### headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA731 data sheet, one can see that when the TPA731 is operating from a 5-V supply into an 8-Ω speaker that 700 mW peaks are available. Converting watts to dB:

$$P_{dB} = 10\,\mathrm{Log}\frac{P_W}{P_{ref}} = 10\mathrm{Log}\,\frac{700\ \mathrm{mW}}{1\ \mathrm{W}} = -1.5\ \mathrm{dB}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

−1.5 dB − 15 dB = −16.5 (15 dB headroom)

−1.5 dB − 12 dB = −13.5 (12 dB headroom)

−1.5 dB − 9 dB = −10.5 (9 dB headroom)

−1.5 dB − 6 dB = −7.5 (6 dB headroom)

−1.5 dB − 3 dB = −4.5 (3 dB headroom)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref}$$

= 22 mW (15 dB headroom)

= 44 mW (12 dB headroom)

= 88 mW (9 dB headroom)

= 175 mW (6 dB headroom)

= 350 mW (3 dB headroom)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 700 mW of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 8-Ω system, the internal dissipation in the TPA731 and maximum ambient temperatures is shown in Table 2.

**Table 2. TPA731 Power Rating, 5-V, 8-Ω, BTL**

| PEAK OUTPUT POWER (mW) | AVERAGE OUTPUT POWER | POWER DISSIPATION (mW) | D PACKAGE (SOIC) | DGN PACKAGE (MSOP) |
|---|---|---|---|---|
| | | | MAXIMUM AMBIENT TEMPERATURE | MAXIMUM AMBIENT TEMPERATURE |
| 700 | 700 mW | 675 | 34°C | 110°C |
| 700 | 350 mW (3 dB) | 595 | 47°C | 115°C |
| 700 | 176 mW (6 dB) | 475 | 68°C | 122°C |
| 700 | 88 mW (9 dB) | 350 | 89°C | 125°C |
| 700 | 44 mW (12 dB) | 225 | 111°C | 125°C |

Table 2 shows that the TPA731 can be used to its full 700-mW rating without any heat sinking in still air up to 110°C and 34°C for the DGN package (MSOP) and D package (SOIC) respectively.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPA731D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TPA731 | Samples |
| TPA731DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TPA731 | Samples |
| TPA731DGN | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AJC | Samples |
| TPA731DGNG4 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AJC | Samples |
| TPA731DGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AJC | Samples |
| TPA731DGNRG4 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AJC | Samples |
| TPA731DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TPA731 | Samples |
| TPA731DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TPA731 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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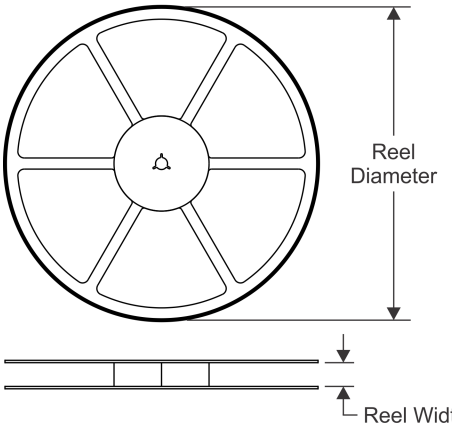
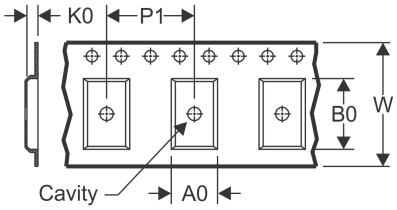
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

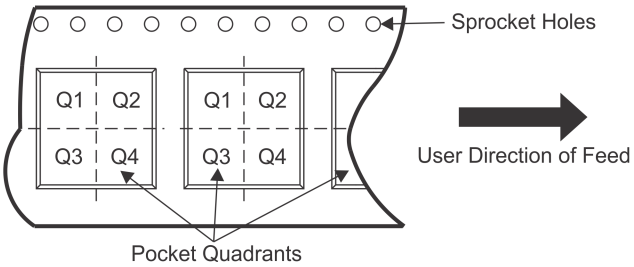



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

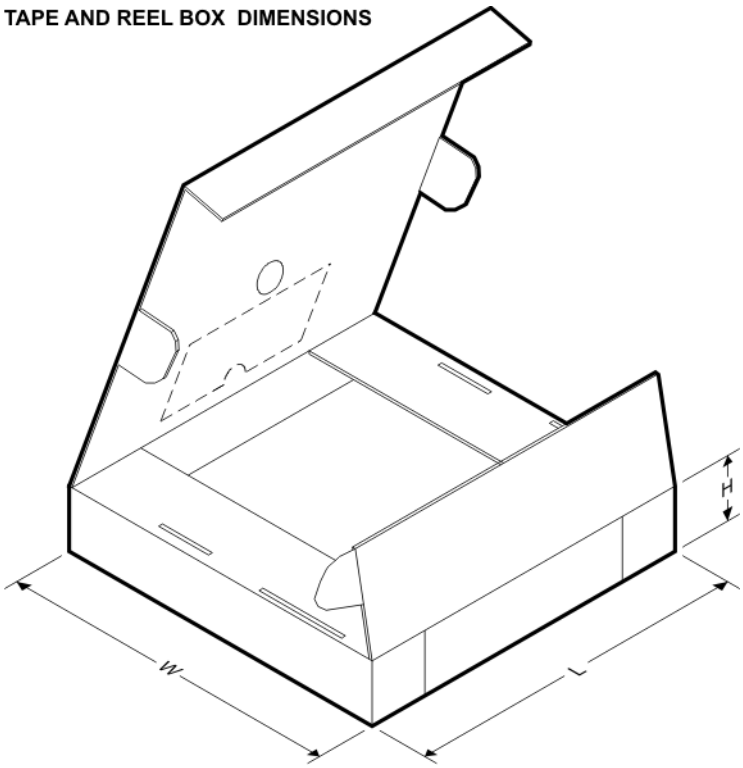
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPA731DGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPA731DGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPA731DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

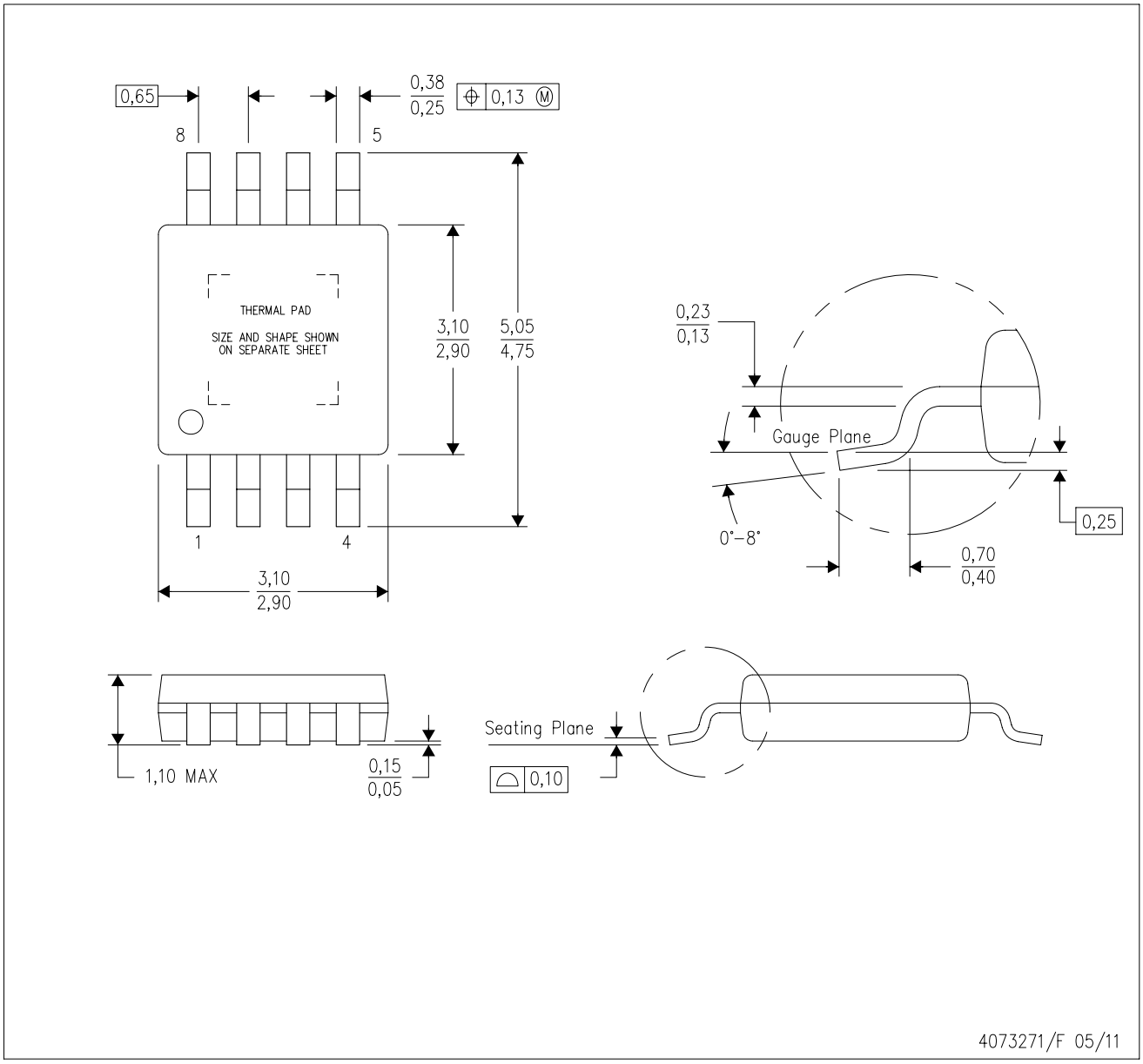
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPA731DGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TPA731DGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPA731DR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-187 variation AA-T

**PowerPAD is a trademark of Texas Instruments.**

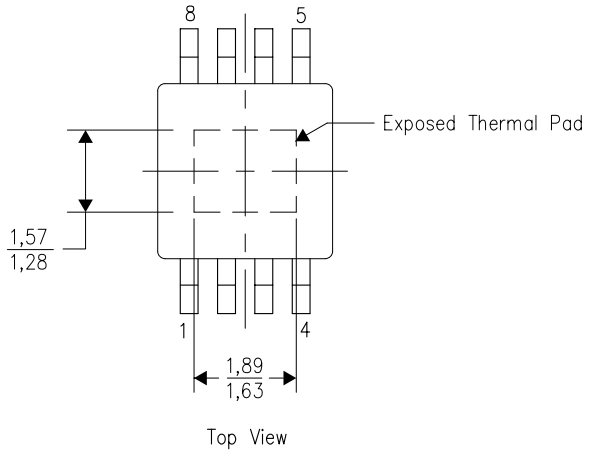
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



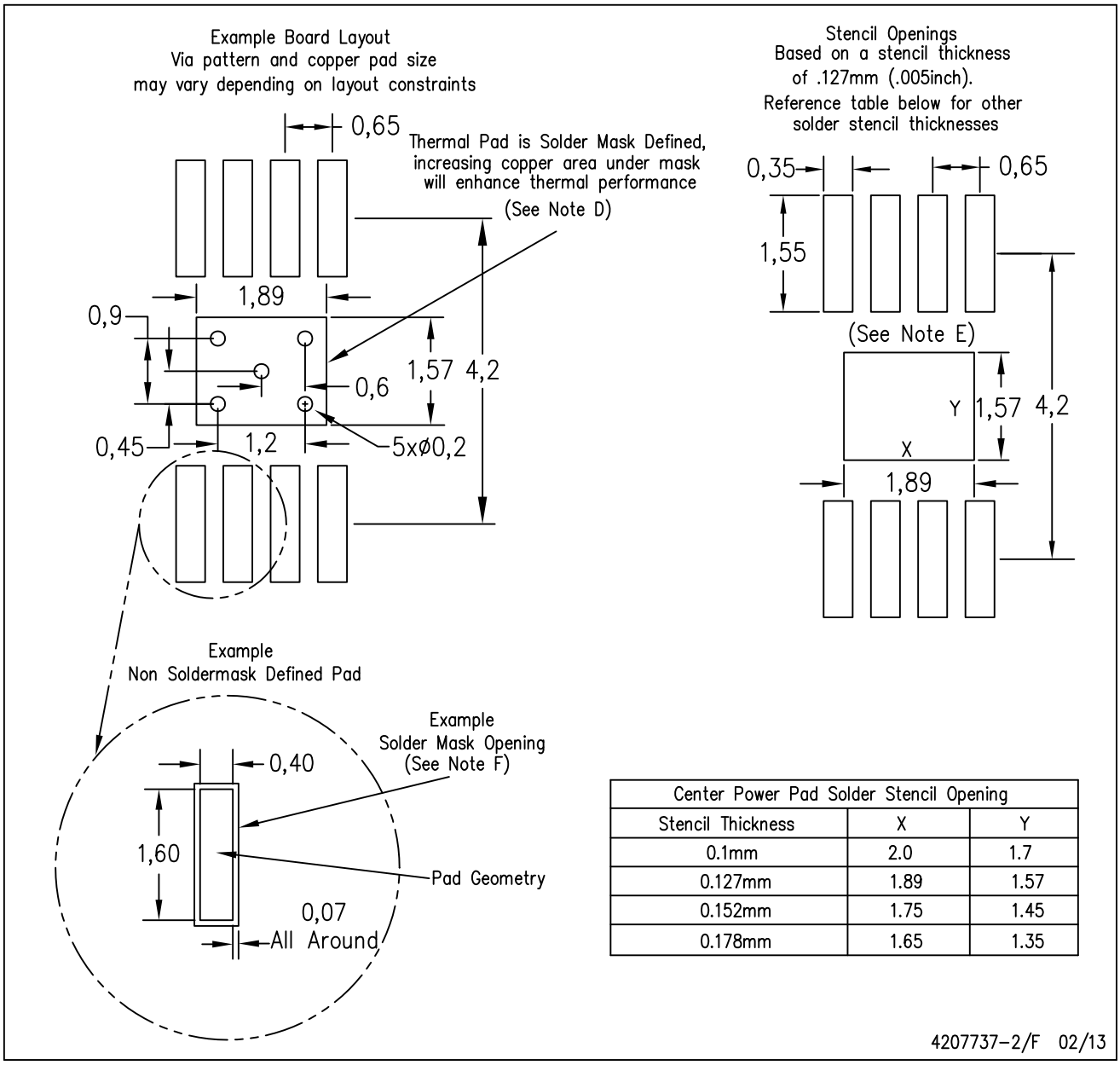

Exposed Thermal Pad Dimensions

4206323-2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

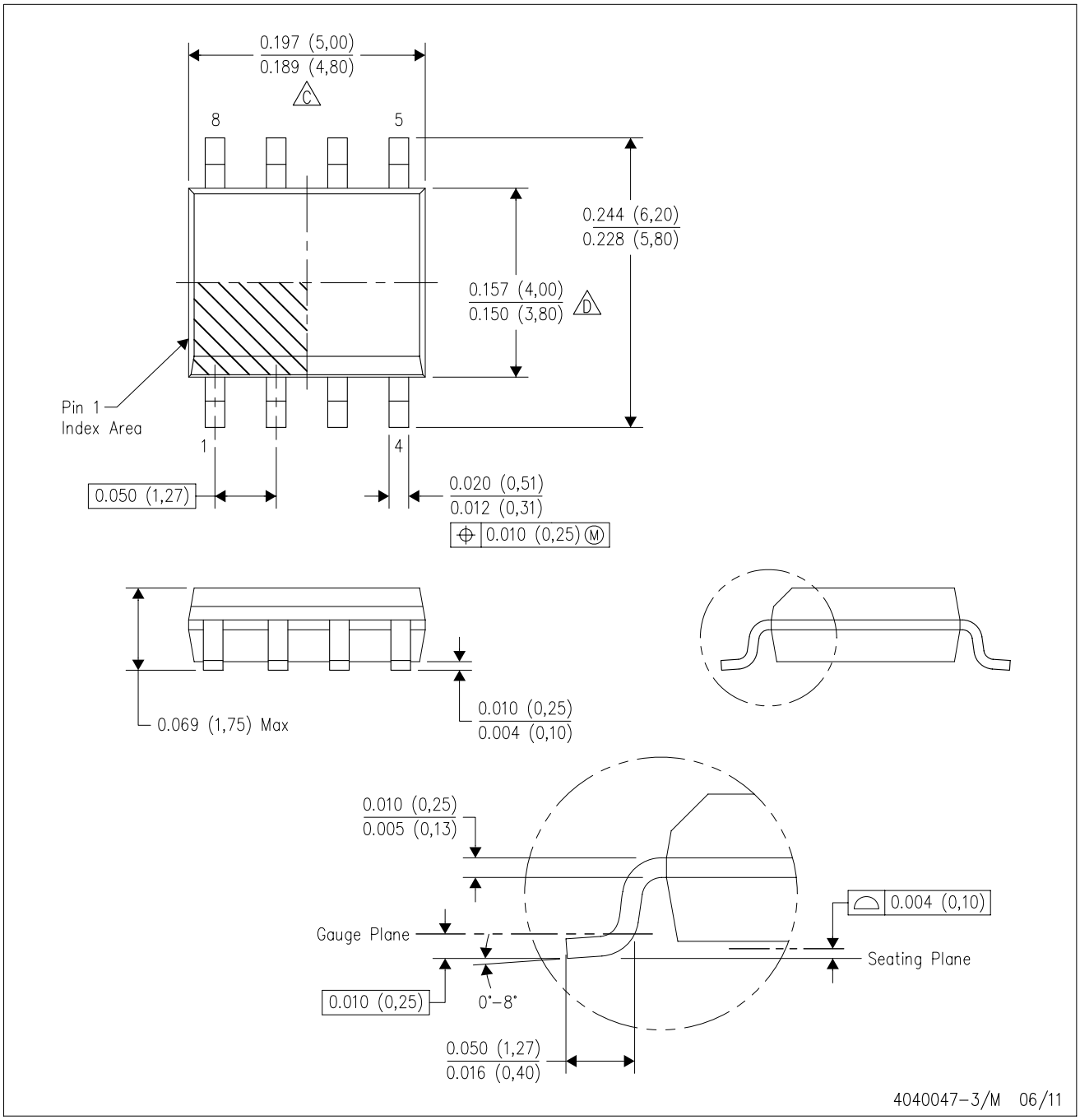



| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.0 | 1.7 |
| 0.127mm | 1.89 | 1.57 |
| 0.152mm | 1.75 | 1.45 |
| 0.178mm | 1.65 | 1.35 |

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

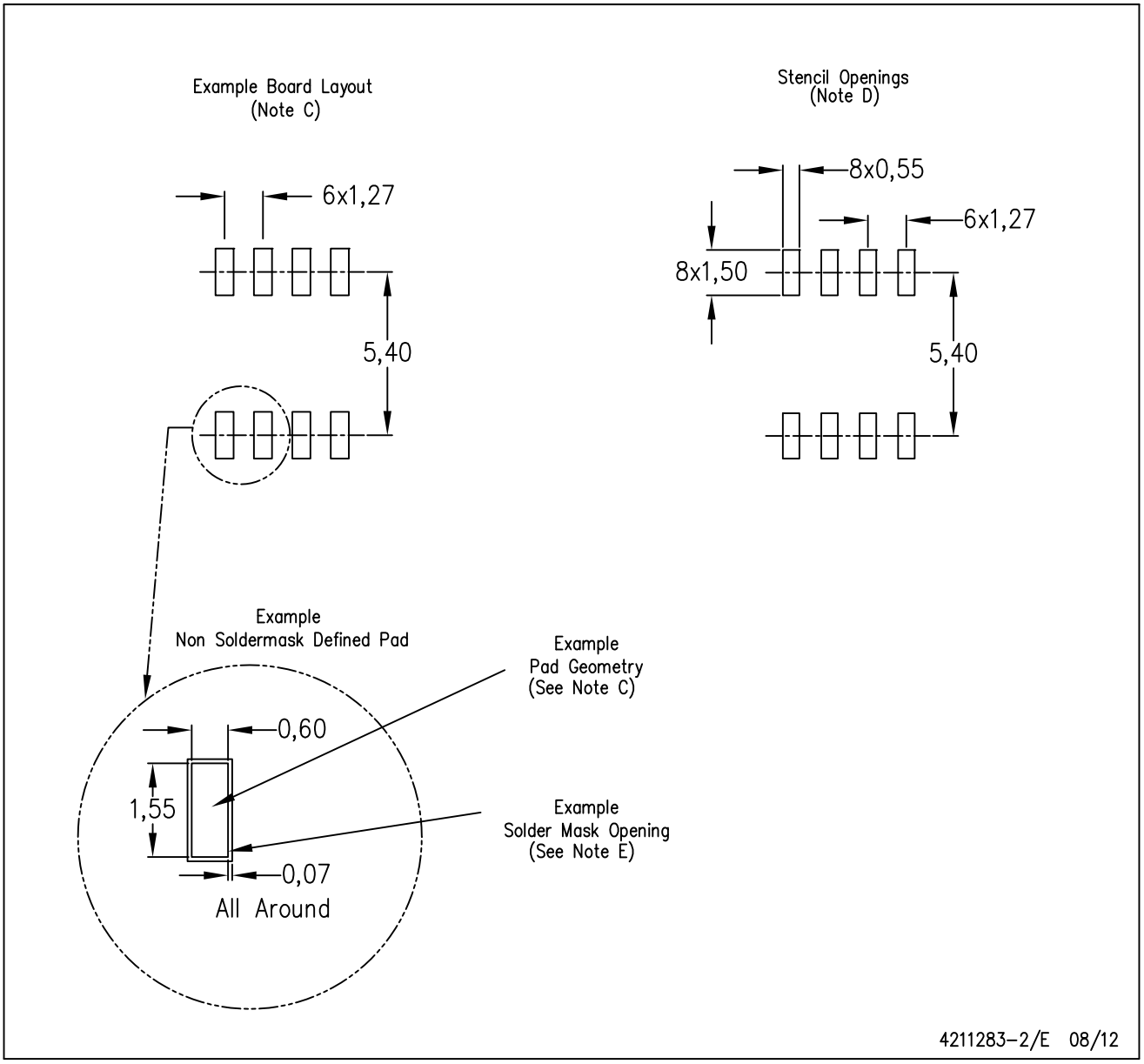
**PowerPAD is a trademark of Texas Instruments**

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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