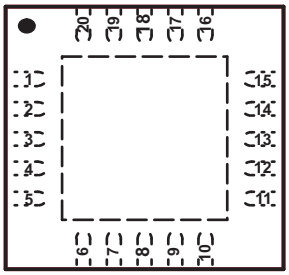
80-mW DIRECTPATH™ STEREO HEADPHONE DRIVER

FEATURES

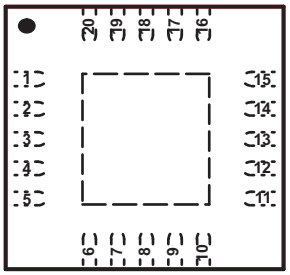
- **Space Saving Packages**
  - **20-Pin, 4 mm × 4 mm Thin QFN**
    - **TPA4411 – Thermally Optimized PowerPAD™ Package**
    - **TPA4411M – Thermally Enhanced PowerPAD™ Package**
  - **16-Ball, 2.18 mm × 2.18 mm WCSP**
- **Ground-Referenced Outputs Eliminate DC-Bias Voltages on Headphone Ground Pin**
  - **No Output DC-Blocking Capacitors**
    - **Reduced Board Area**
    - **Reduced Component Cost**
    - **Improved THD+N Performance**
    - **No Degradation of Low-Frequency Response Due to Output Capacitors**
- **Wide Power Supply Range: 1.8 V to 4.5 V**
- **80-mW/Ch Output Power into 16-Ω at 4.5 V**
- **Independent Right and Left Channel Shutdown Control**
- **Short-Circuit and Thermal Protection**
- **Pop Reduction Circuitry**

APPLICATIONS

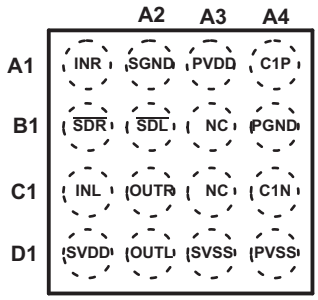
- **Notebook Computers**
- **CD / MP3 Players**
- **Smart Phones**
- **Cellular Phones**
- **PDAs**



TPA4411RTJ



TPA4411MRTJ



TPA4411YZH

DESCRIPTION

The TPA4411 and TPA4411M are stereo headphone drivers designed to allow the removal of the output DC-blocking capacitors for reduced component count and cost. The TPA4411 and TPA4411M are ideal for small portable electronics where size and cost are critical design parameters.

The TPA4411 and TPA4411M are capable of driving 80 mW into a 16-Ω load at 4.5 V. Both TPA4411 and TPA4411M have a fixed gain of –1.5 V/V and headphone outputs that have ±8-kV IEC ESD protection. The TPA4411 and TPA4411M have independent shutdown control for the right and left audio channels.

The TPA4411 is available in a 2.18 mm × 2.18 mm WCSP and 4 mm × 4 mm Thin QFN packages. The TPA4411M is available in a 4 mm × 4 mm Thin QFN package. The TPA4411RTJ package is a thermally optimized PowerPAD™ package allowing the maximum amount of thermal dissipation and the TPA4411MRTJ is a thermally enhanced PowerPAD package designed to match competitive package footprints.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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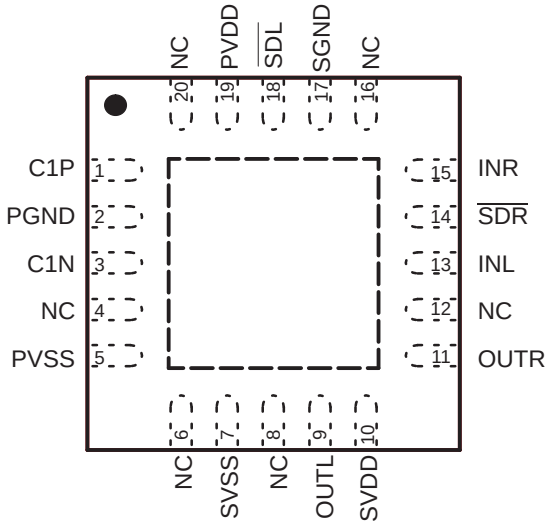
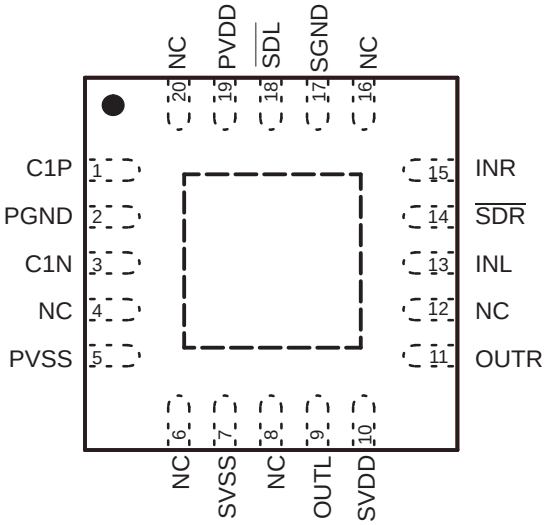
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

RTJ (QFN) PACKAGE
(TOP VIEW)



TPA4411RTJ

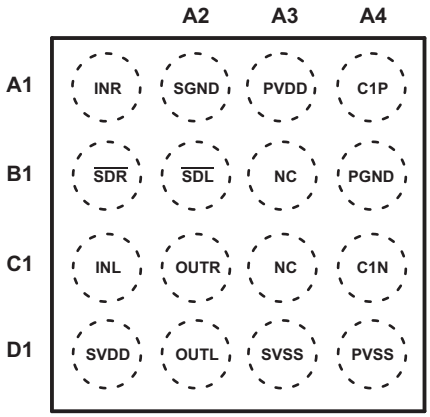
NC − No internal connection



TPA4411MRTJ

NC − No internal connection

YZH (WCSP) PACKAGE
(TOP VIEW)



TPA4411YZH

NC - No internal connection

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TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	QFN	WCSP		
C1P	1	A4	I/O	Charge pump flying capacitor positive terminal
PGND	2	B4	I	Power ground, connect to ground.
C1N	3	C4	I/O	Charge pump flying capacitor negative terminal
NC	4, 6, 8, 12, 16, 20	B3, C3		No connection
PVSS	5	D4	O	Output from charge pump.
SVSS	7	D3	I	Amplifier negative supply, connect to PVSS via star connection.
OUTL	9	D2	O	Left audio channel output signal
SVDD	10	D1	I	Amplifier positive supply, connect to PVDD via star connection.
OUTR	11	C2	O	Right audio channel output signal
INL	13	C1	I	Left audio channel input signal
$\overline{SDR}$	14	B1	I	Right channel shutdown, active low logic.
INR	15	A1	I	Right audio channel input signal
SGND	17	A2	I	Signal ground, connect to ground.
$\overline{SDL}$	18	B2	I	Left channel shutdown, active low logic.
PVDD	19	A3	I	Supply voltage, connect to positive supply.
Exposed Pad		-		Exposed pad must be soldered to a floating plane. Do NOT connect to power or ground.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)

		VALUE / UNIT
	Supply voltage, AVDD, PVDD	–0.3 V to 5.5 V
V_I	Input voltage	–0.3 V to V_{DD} + 0.3 V
	Output Continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature range	–40°C to 85°C
T_J	Operating junction temperature range	–40°C to 150°C
T_{stg}	Storage temperature range	–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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DISSIPATION RATINGS TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1)	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RTJ (TPA4411)	5200 mW	41.6 mW/°C	3120 mW	2700 mW
RTJ (TPA4411M)	3450 mW	34.5 mW/°C	1898 mW	1380 mW
YZH	1200 mW	9.21 mW/°C	690 mW	600 mW

(1) Derating factor measured with High K board.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES(1)	PART NUMBER	SYMBOL
–40°C to 85°C	20-pin, 4 mm × 4 mm QFN	TPA4411RTJ(2)	AKQ
	20-pin, 4 mm × 4 mm QFN	TPA4411MRTJ(2)	BPB
	16-ball, 2.18 mm × 2.18 mm WSCP	TPA4411YZH	AKT

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The RTJ package is only available taped and reeled. To order, add the suffix "R" to the end of the part number for a reel of 3000, or add the suffix "T" to the end of the part number for a reel of 250 (e.g., TPA4411RTJR).

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
	Supply voltage, AVDD, PVDD		1.8	4.5(1)	V
V_{IH}	High-level input voltage	$\overline{SDL}$, $\overline{SDR}$	1.5		V
V_{IL}	Low-level input voltage	$\overline{SDL}$, $\overline{SDR}$		0.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) Device can shut down for VDD > 4.5 V to prevent damage to the device.

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
|VOS|	Output offset voltage	V_{DD} = 1.8 V to 4.5 V, Inputs grounded			8	mV
PSRR	Power Supply Rejection Ratio	V_{DD} = 1.8 V to 4.5 V	–69	–80		dB
V_{OH}	High-level output voltage	V_{DD} = 3 V, R_L = 16 Ω	2.2			V
V_{OL}	Low-level output voltage	V_{DD} = 3 V, R_L = 16 Ω			–1.1	V
$\|I_{IH}\|$	High-level input current ($\overline{SDL}$, $\overline{SDR}$)	V_{DD} = 4.5 V, $V_I = V_{DD}$			1	µA
$\|I_{IL}\|$	Low-level input current ($\overline{SDL}$, $\overline{SDR}$)	V_{DD} = 4.5 V, V_I = 0 V			1	µA
I_{DD}	Supply Current	V_{DD} = 1.8 V, No load, $\overline{SDL}$= $\overline{SDR}$ = V_{DD}		5.3	6.5	mA
		V_{DD} = 3 V, No load, $\overline{SDL}$ = $\overline{SDR}$ = V_{DD}		6.5	8.0	
		V_{DD} = 4.5 V, No load, $\overline{SDL}$ = $\overline{SDR}$ = V_{DD}		8.0	10.0	
		Shutdown mode, V_{DD} = 1.8 V to 4.5 V			1	µA

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OPERATING CHARACTERISTICS

V_{DD} = 3 V , T_A = 25°C, R_L = 16 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (Outputs In Phase)	THD = 1%, V_{DD} = 3 V, f = 1 kHz		50		mW
		THD = 1%, V_{DD} = 4.5 V, f = 1 kHz		100		
		THD = 1%, V_{DD} = 3 V, f = 1 kHz, R_L = 32 Ω		50		
THD+N	Total harmonic distortion plus noise	P_O = 25 mW, f = 1 kHz		0.054%		
		P_O = 25 mW, f = 20 kHz		0.010%		
	Crosstallk	P_O = 20 mW, f = 1 kHz		–83		dB
k_{SVR}	Supply ripple rejection ratio	200-mV_{pp} ripple, f = 217 Hz		–82.5		dB
		200-mV_{pp} ripple, f = 1 kHz		–70.4		
		200-mV_{pp} ripple, f = 20 kHz		–45.1		
A_v	Closed-loop voltage gain		–1.45	–1.5	–1.55	V/V
ΔA_v	Gain matching			1%		
	Slew rate			2.2		V/µs
	Maximum capacitive load			400		pF
V_n	Noise output voltage			10		μV_{RMS}
	Electrostatic discharge, IEC	OUTR, OUTL		±8		kV
f_{osc}	Charge pump switching frequency		280	320	420	kHz
	Start-up time from shutdown			450		µs
	Input impedance		12	15	18	kΩ
SNR	Signal-to-noise ratio	P_o = 40 mW (THD+N = 0.1%)		98		dB
	Thermal shutdown	Threshold	150		170	°C
		Hysteresis		15		°C

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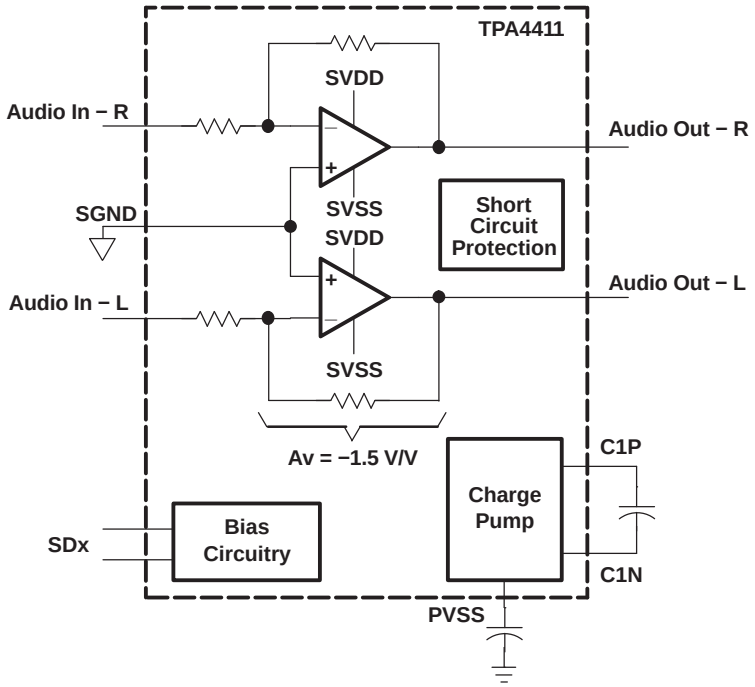
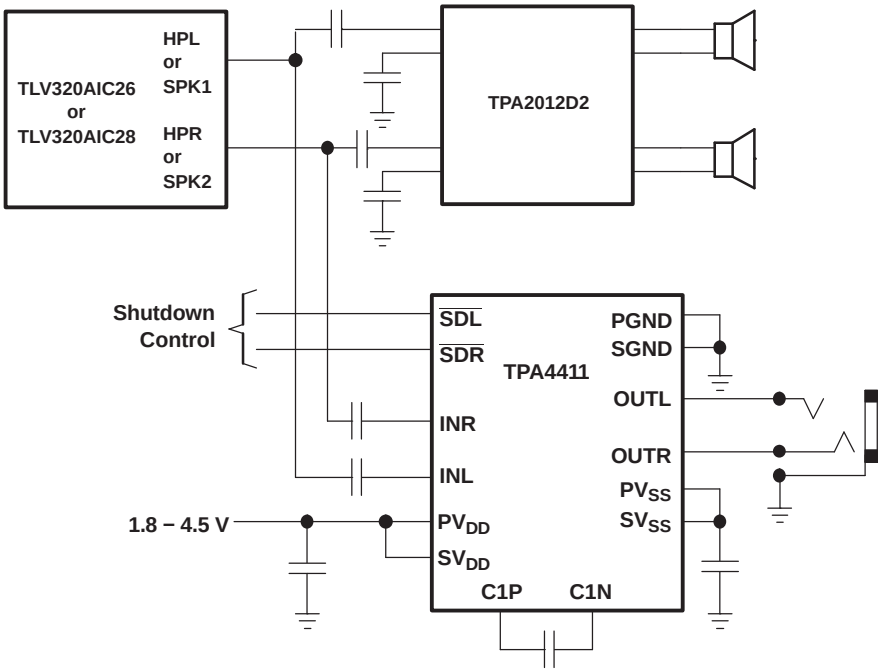
Functional Block Diagram



APPLICATION CIRCUIT



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TYPICAL CHARACTERISTICS

$C_{(PUMP)} = C_{(PVSS)} = 2.2\ \mu F$, $C_{IN} = 1\ \mu F$ (unless otherwise noted)

Table of Graphs

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Total harmonic distortion + noise	vs Output power	1–24
Total harmonic distortion + noise	vs Frequency	25–32
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TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

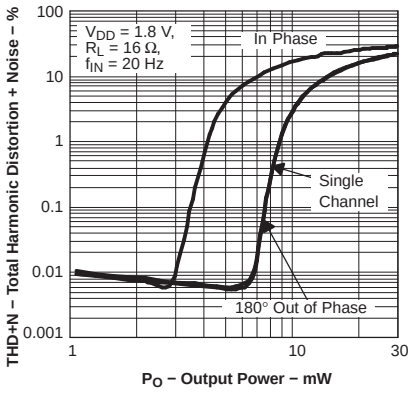

Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

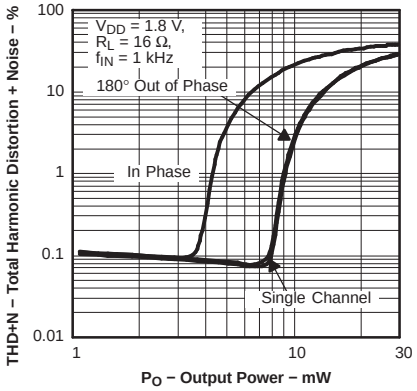

Figure 2.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

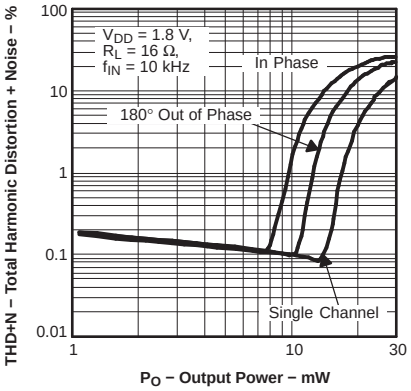

Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

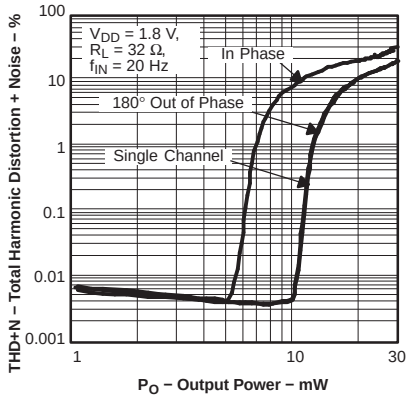

Figure 4.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

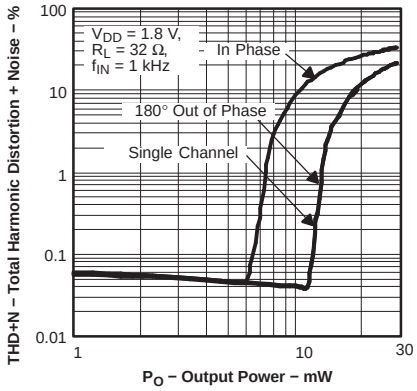

Figure 5.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

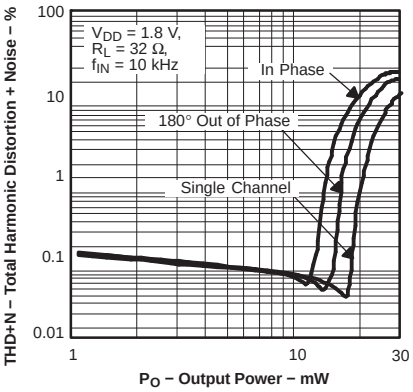

Figure 6.

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TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

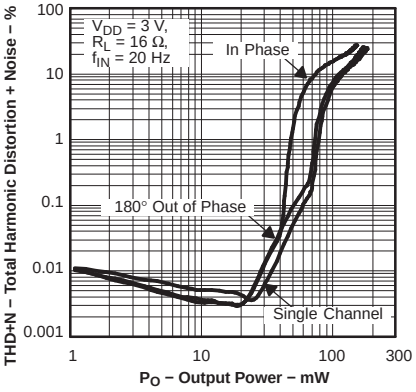

Figure 7.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

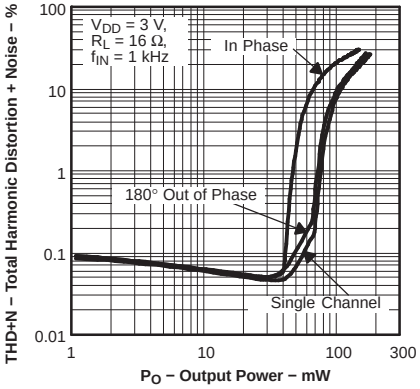

Figure 8.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

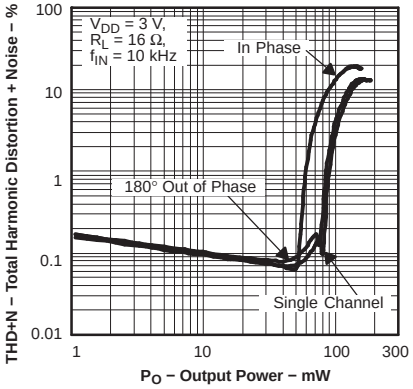

Figure 9.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

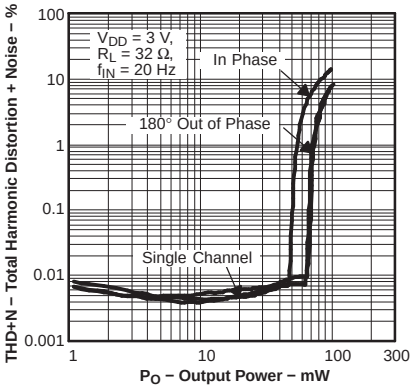

Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

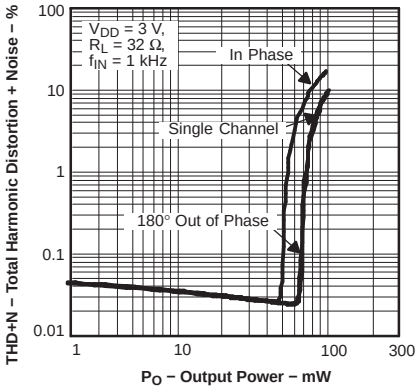

Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

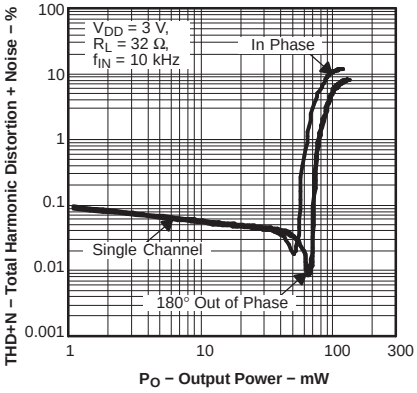

Figure 12.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

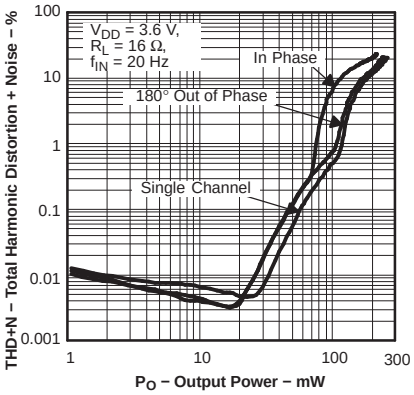

Figure 13.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

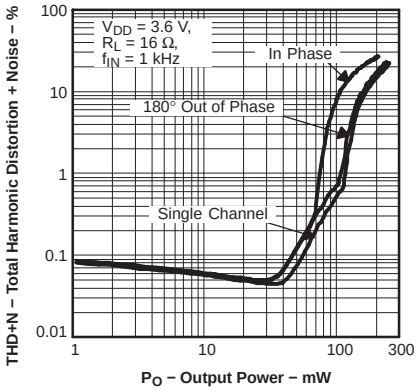

Figure 14.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

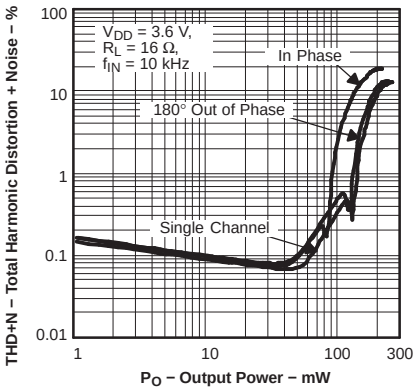

Figure 15.

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TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

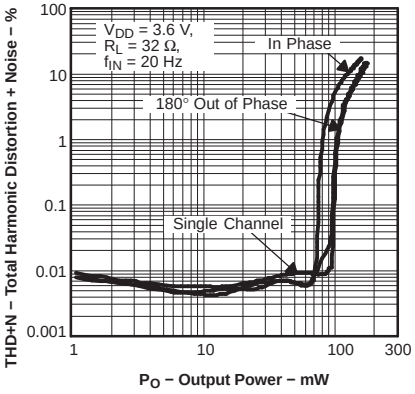

Figure 16.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

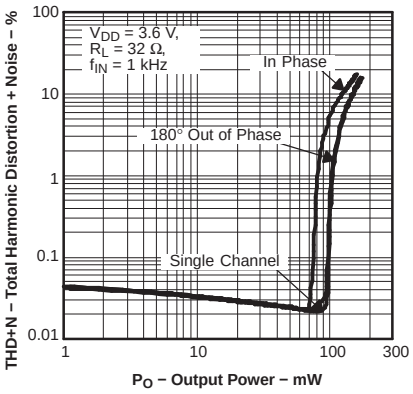

Figure 17.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

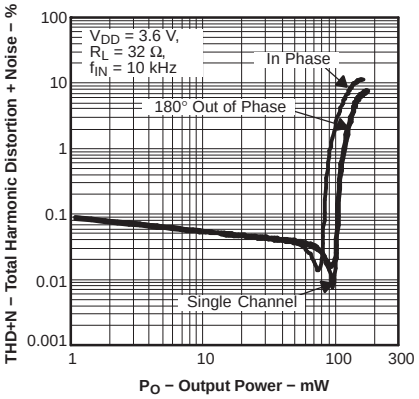

Figure 18.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

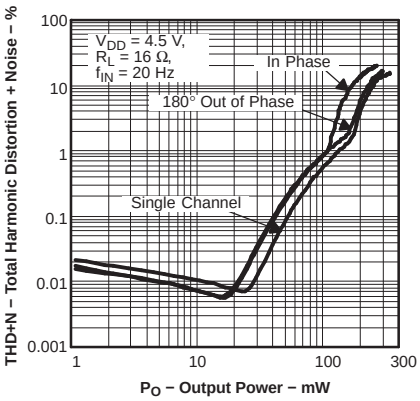

Figure 19.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

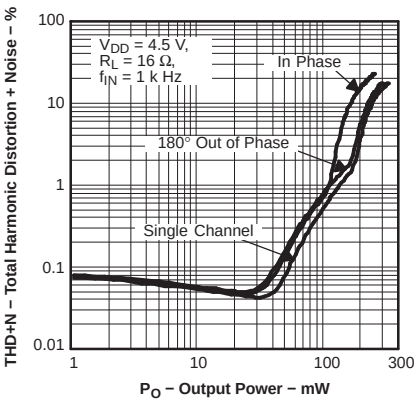

Figure 20.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

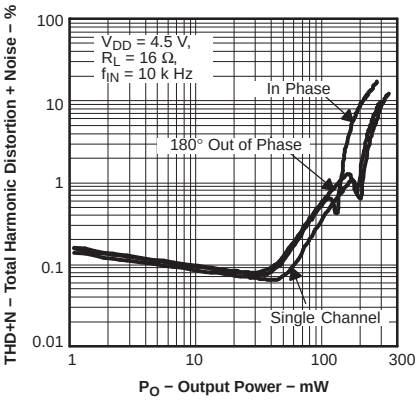

Figure 21.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

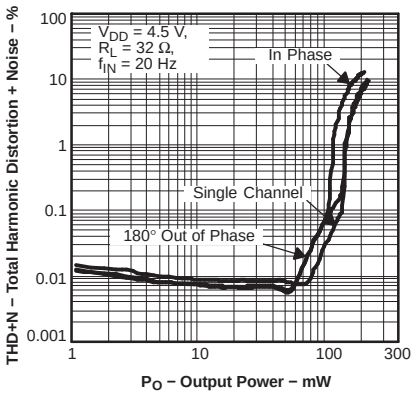

Figure 22.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

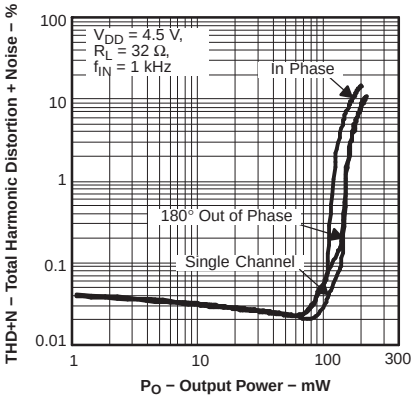

Figure 23.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

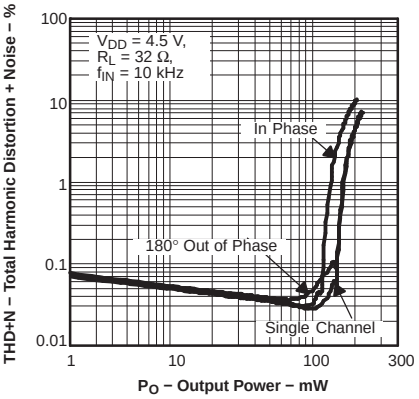

Figure 24.

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TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

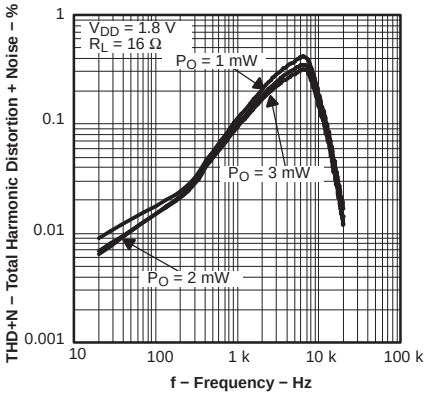

Figure 25.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

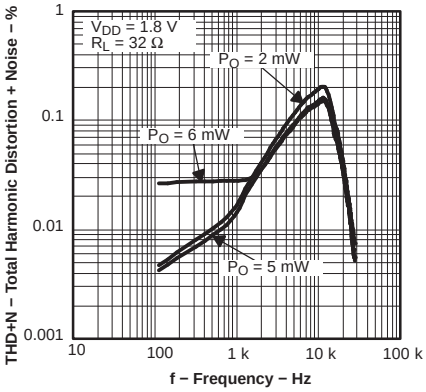

Figure 26.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

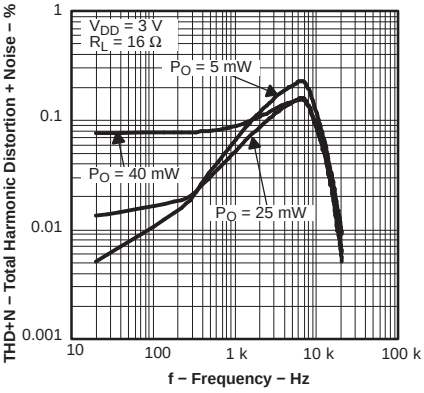

Figure 27.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

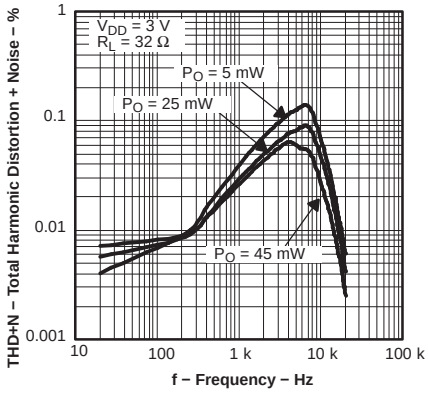

Figure 28.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

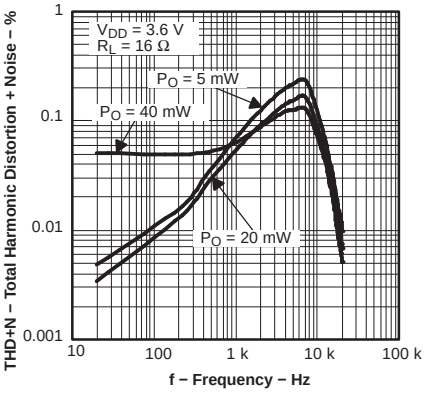

Figure 29.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

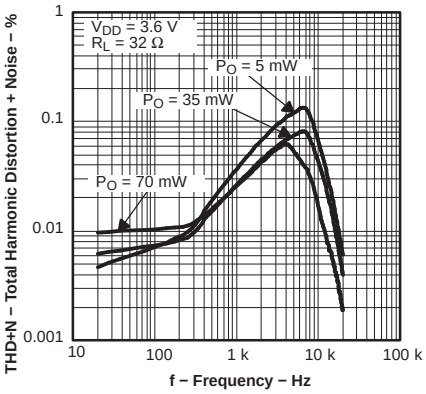

Figure 30.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

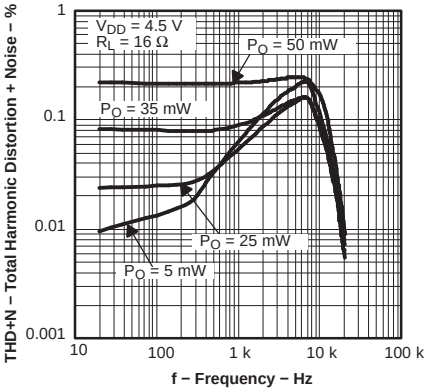

Figure 31.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

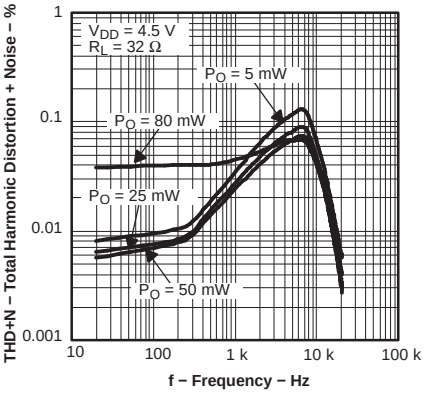

Figure 32.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

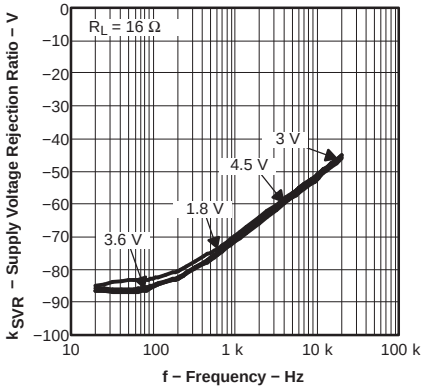

Figure 33.

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SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

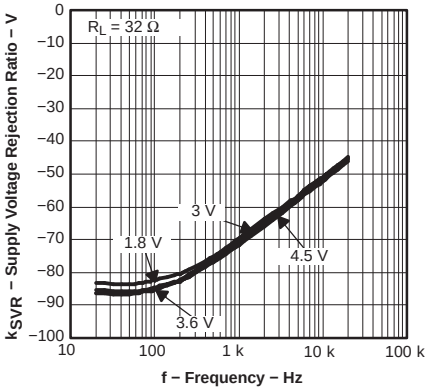

Figure 34.

POWER DISSIPATION vs OUTPUT POWER

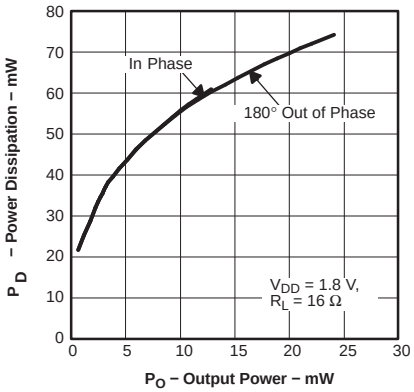

Figure 35.

POWER DISSIPATION vs OUTPUT POWER

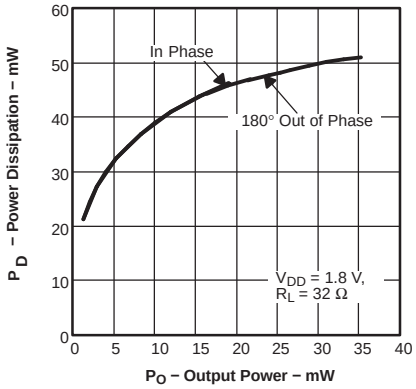

Figure 36.

POWER DISSIPATION vs OUTPUT POWER

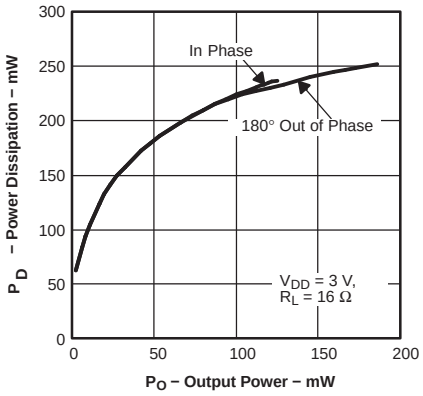

Figure 37.

POWER DISSIPATION vs OUTPUT POWER

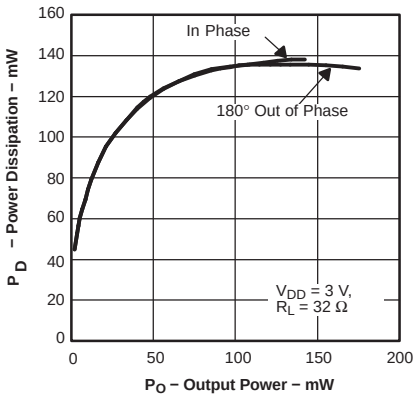

Figure 38.

POWER DISSIPATION vs OUTPUT POWER

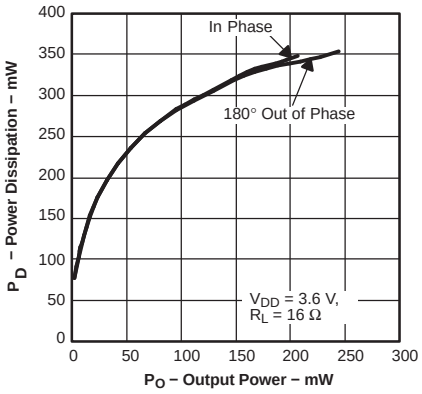

Figure 39.

POWER DISSIPATION vs OUTPUT POWER

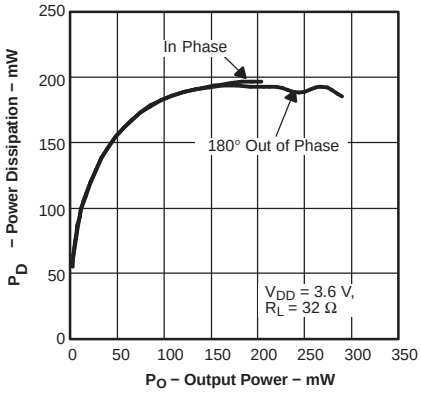

Figure 40.

POWER DISSIPATION vs OUTPUT POWER

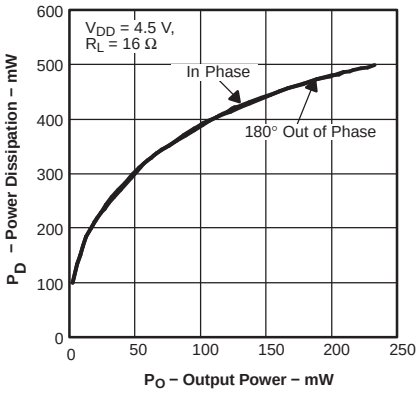

Figure 41.

POWER DISSIPATION vs OUTPUT POWER

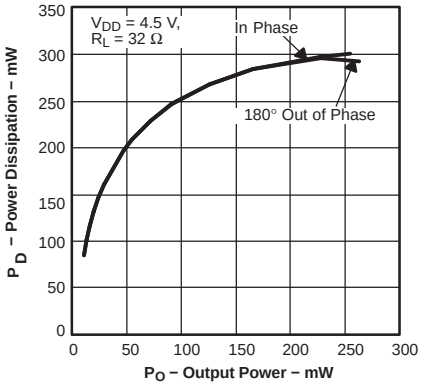

Figure 42.

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CROSSTALK vs FREQUENCY

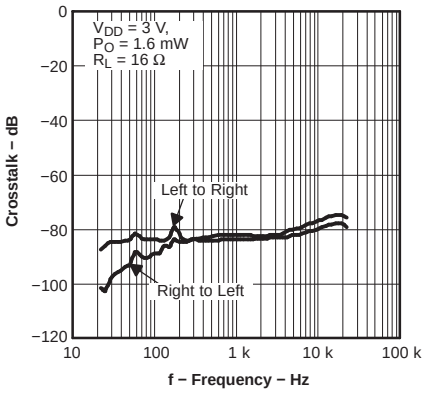

Figure 43.

CROSSTALK vs FREQUENCY

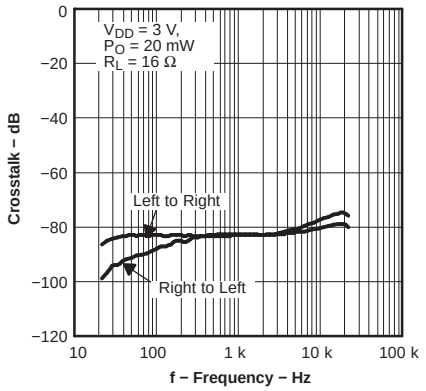

Figure 44.

CROSSTALK vs FREQUENCY

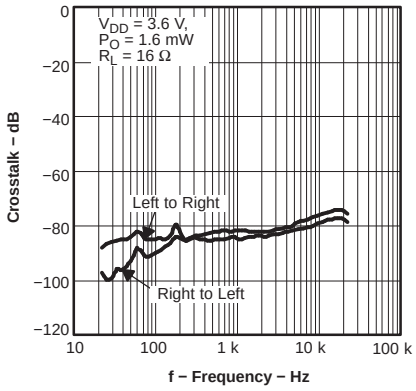

Figure 45.

CROSSTALK vs FREQUENCY

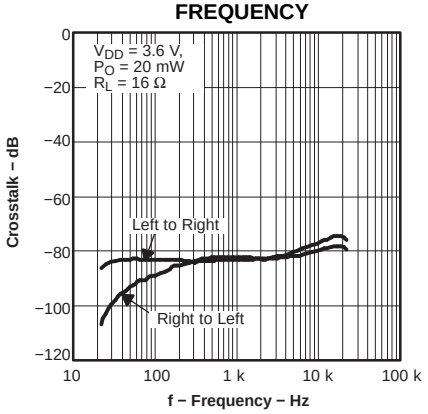

Figure 46.

OUTPUT POWER vs SUPPLY VOLTAGE

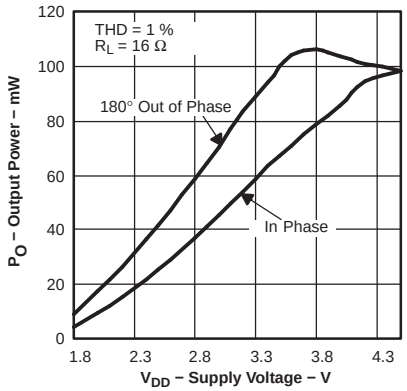

Figure 47.

OUTPUT POWER vs SUPPLY VOLTAGE

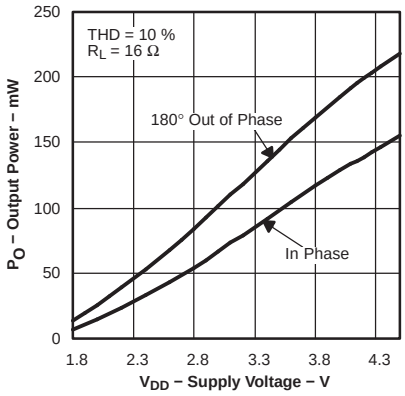

Figure 48.

OUTPUT POWER vs SUPPLY VOLTAGE

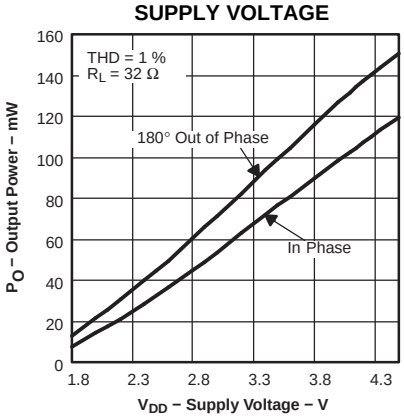

Figure 49.

OUTPUT POWER vs SUPPLY VOLTAGE

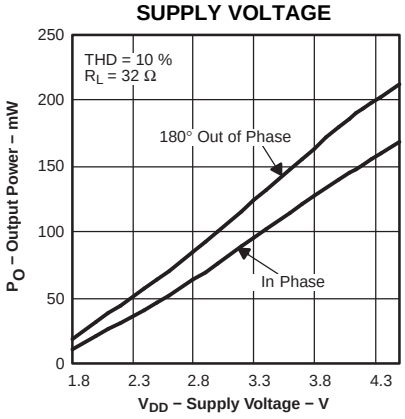

Figure 50.

QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

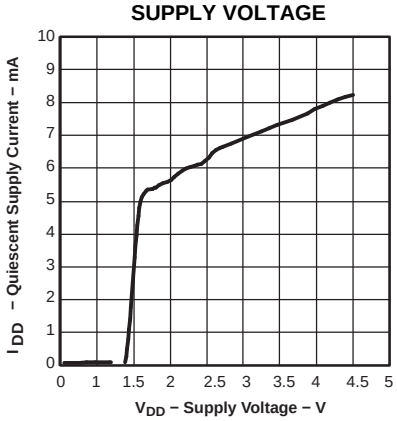

Figure 51.

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OUTPUT POWER vs LOAD RESISTANCE

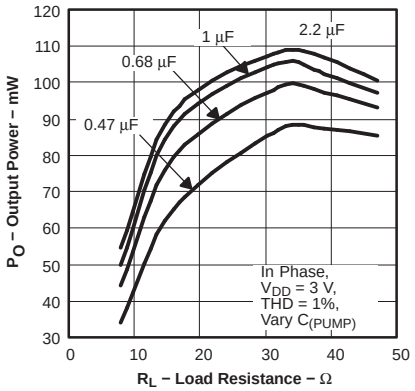

Figure 52.

OUTPUT POWER vs LOAD RESISTANCE

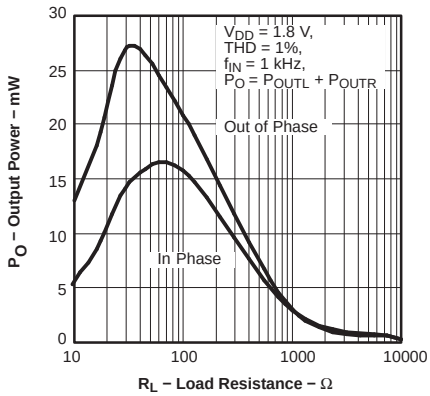

Figure 53.

OUTPUT POWER vs LOAD RESISTANCE

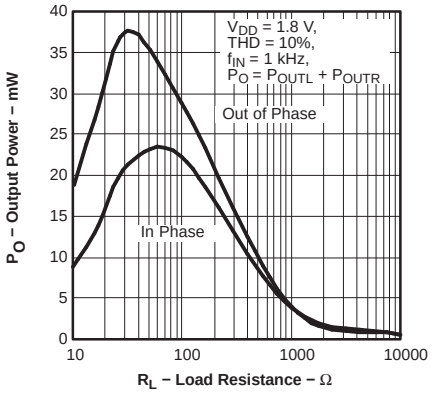

Figure 54.

OUTPUT POWER vs LOAD RESISTANCE

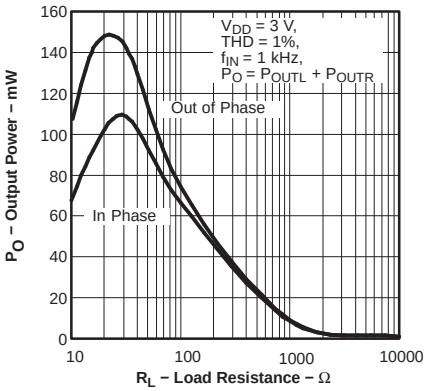

Figure 55.

OUTPUT POWER vs LOAD RESISTANCE

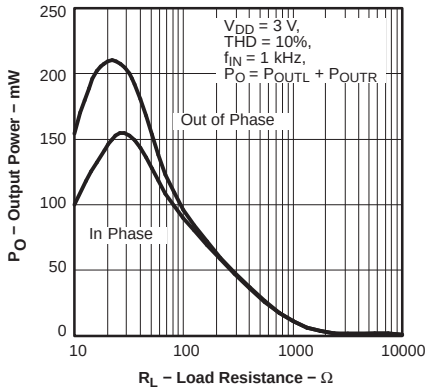

Figure 56.

OUTPUT POWER vs LOAD RESISTANCE

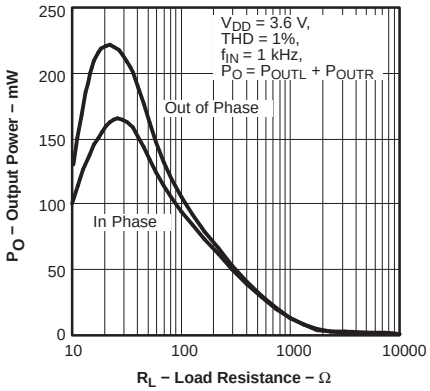

Figure 57.

OUTPUT POWER vs LOAD RESISTANCE

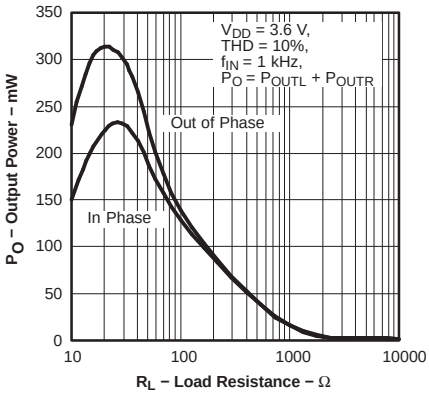

Figure 58.

OUTPUT POWER vs LOAD RESISTANCE

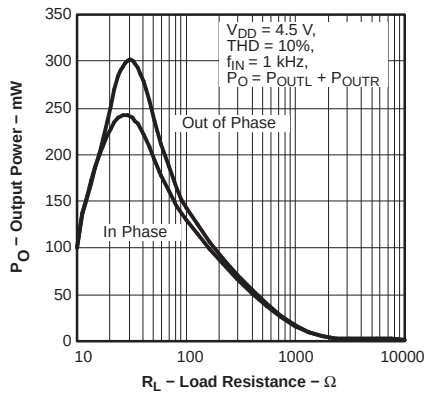

Figure 59.

OUTPUT POWER vs LOAD RESISTANCE

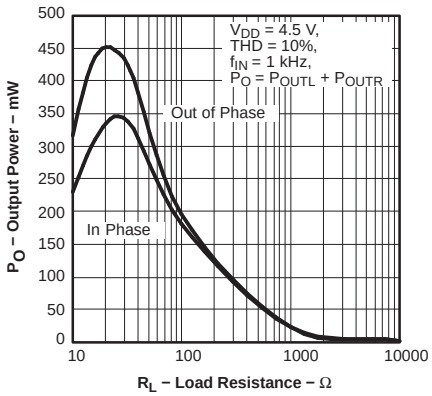

Figure 60.

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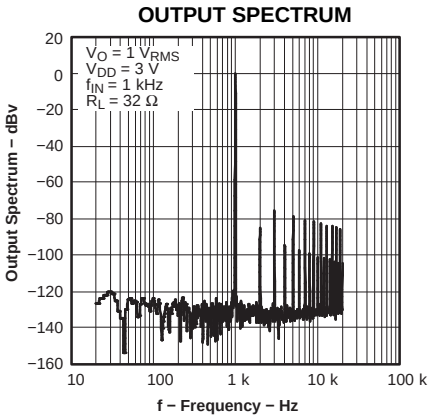

Figure 61.

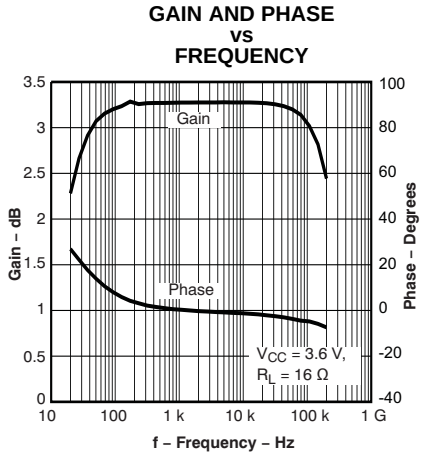

Figure 62.

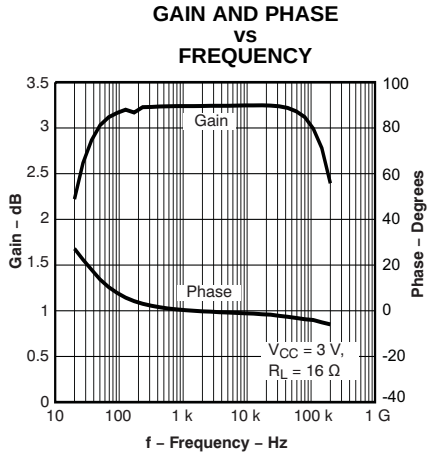

Figure 63.

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APPLICATION INFORMATION

Headphone Amplifiers

Single-supply headphone amplifiers typically require dc-blocking capacitors. The capacitors are required because most headphone amplifiers have a dc bias on the outputs pin. If the dc bias is not removed, the output signal is severely clipped, and large amounts of dc current rush through the headphones, potentially damaging them. The top drawing in Figure 64 illustrates the conventional headphone amplifier connection to the headphone jack and output signal.

DC blocking capacitors are often large in value. The headphone speakers (typical resistive values of 16 Ω or 32 Ω) combine with the dc blocking capacitors to form a high-pass filter. Equation 1 shows the relationship between the load impedance $_L$), the capacitor $_O$), and the cutoff frequency (f_C).

$$f_c = \frac{1}{2\pi R_L C_O} \tag{1}$$

C_O can be determined using Equation 2, where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_c} \tag{2}$$

If f_C is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

Two different headphone amplifier applications are available that allow for the removal of the output dc blocking capacitors. The Capless amplifier architecture is implemented in the same manner as the conventional amplifier with the exception of the headphone jack shield pin. This amplifier provides a reference voltage, which is connected to the headphone jack shield pin. This is the voltage on which the audio output signals are centered. This voltage reference is half of the amplifier power supply to allow symmetrical swing of the output voltages. Do not connect the shield to any GND reference or large currents will result. The scenario can happen if, for example, an accessory other than a floating GND headphone is plugged into the headphone connector. See the second block diagram and waveform in Figure 64.

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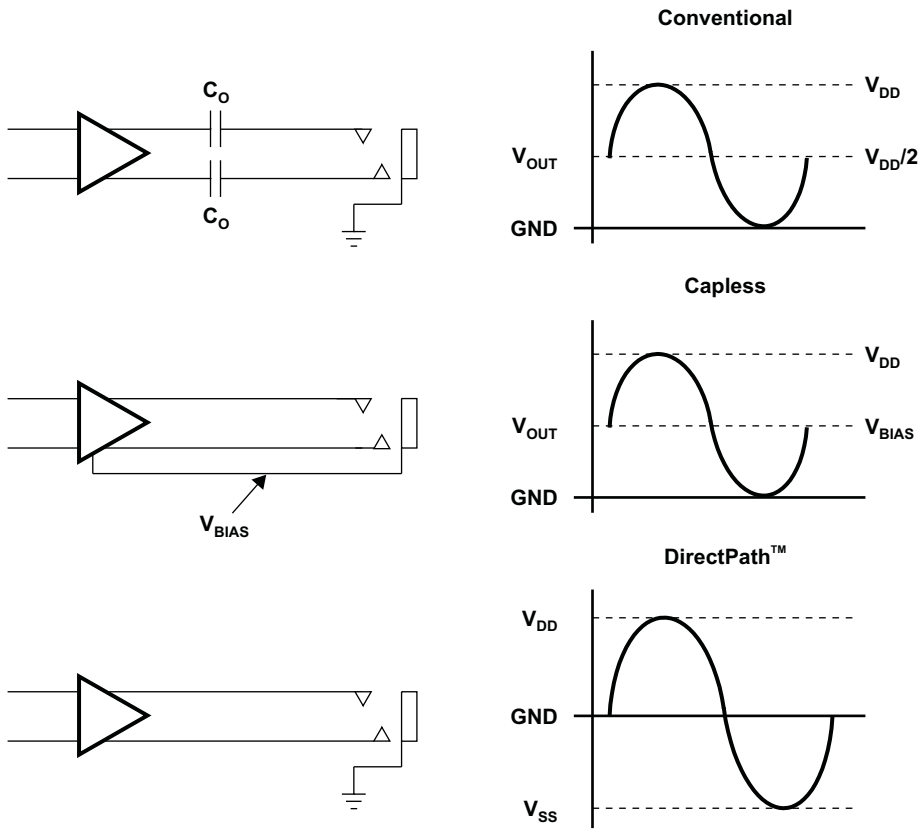

Figure 64. Amplifier Applications

The DirectPath™ amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. The DirectPath™ amplifier requires no output dc blocking capacitors, and does not place any voltage on the sleeve. The bottom block diagram and waveform of Figure 64 illustrate the ground-referenced headphone architecture. This is the architecture of the TPA4411.

Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the TPA4411 and TPA4411M. These capacitors block the DC portion of the audio source and allow the TPA4411 and TPA4411M inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input impedance of the TPA4411 and TPA4411M. The cutoff frequency is calculated using Equation 3. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input impedance of the TPA4411 or TPA4411M. Because the gains of both the TPA4411 and TPA4411M are fixed, the input impedance remains a constant value. Using the input impedance value from the operating characteristics table, the frequency and/or capacitance can be determined when one of the two values are given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \tag{3}$$

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Charge Pump Flying Capacitor and PVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 2.2 µF is typical. Capacitor values that are smaller than 2.2 µF can be used, but the maximum output power is reduced and the device may not operate to specifications. Figure 65 through Figure 75 compare the performance of the TPA4411 and TPA4411M with the recommended 2.2-µF capacitors and 1-µF capacitors.

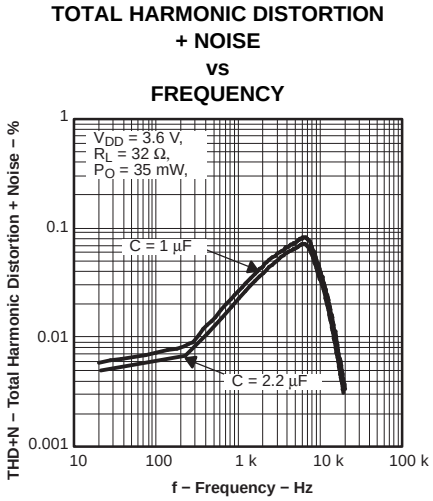

Figure 65.

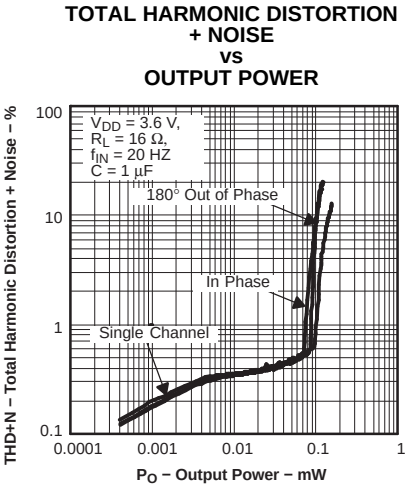

Figure 66.

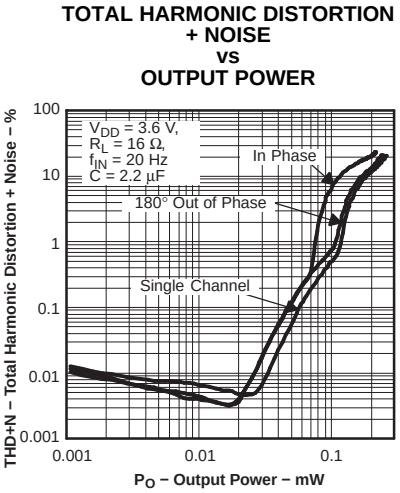

Figure 67.

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TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

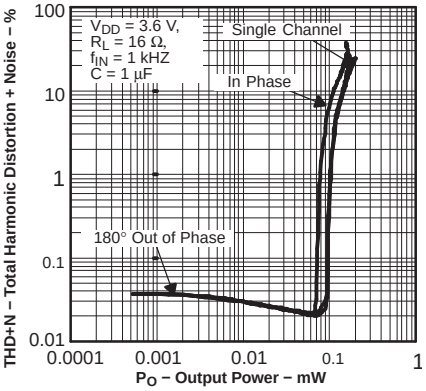

Figure 68.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

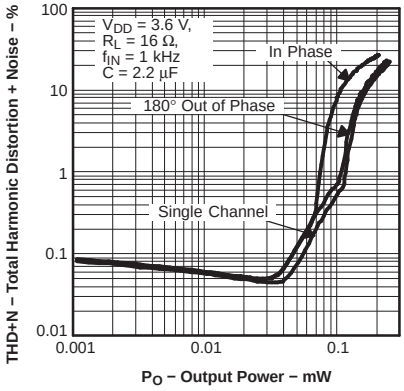

Figure 69.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

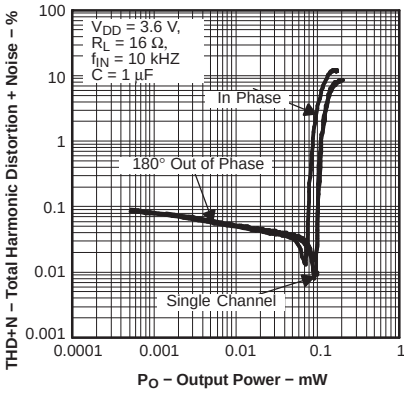

Figure 70.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

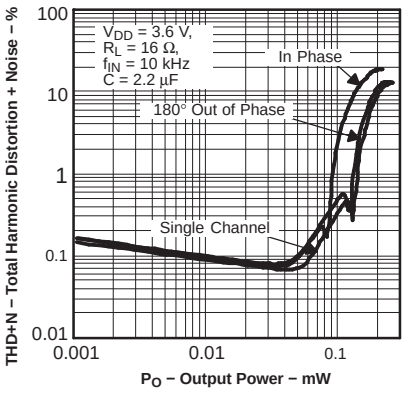

Figure 71.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

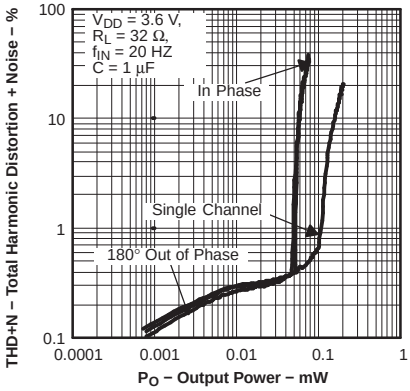

Figure 72.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

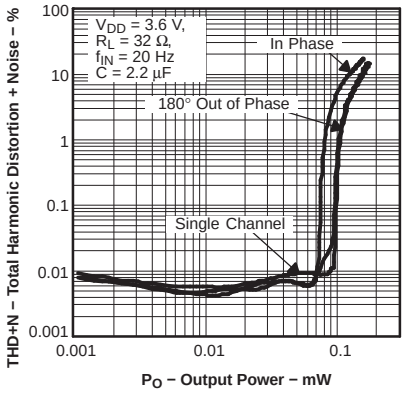

Figure 73.

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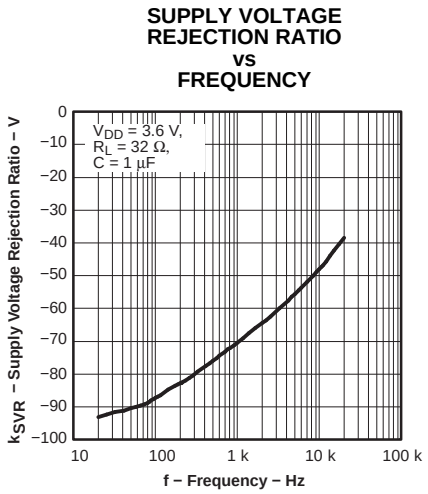

Figure 74.

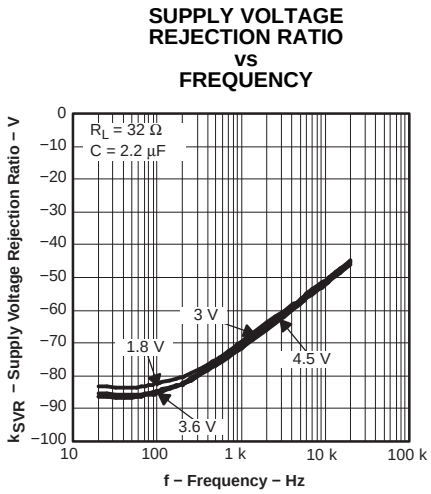

Figure 75.

Decoupling Capacitors

The TPA4411 and TPA4411M are DirectPath™ headphone amplifiers that require adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 2.2 µF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the TPA4411 or TPA4411M is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Supply Voltage Limiting At 4.5 V

The TPA4411 and TPA4411M have a built-in charge pump which serves to generate a negative rail for the headphone amplifier. Because the headphone amplifier operates from a positive voltage and negative voltage supply, circuitry has been implemented to protect the devices in the amplifier from an overvoltage condition. Once the supply is above 4.5 V, the TPA4411 and TPA4411M can shut down in an overvoltage protection mode to prevent damage to the device. The TPA4411 and TPA4411M resume normal operation once the supply is reduced to 4.5 V or lower.

Layout Recommendations

Exposed Pad On TPA4411RTJ and TPA4411MRTJ Package Option

The exposed metal pad on the TPA4411RTJ and TPA4411MRTJ packages must be soldered down to a pad on the PCB in order to maintain reliability. *The pad on the PCB should be allowed to float and not be connected to ground or power*. Connecting this pad to power or ground prevents the device from working properly because it is connected internally to PVSS.

TPA4411RTJ and TPA441MRTJ PowerPAD Sizes

Both the TPA4411 and TPA4411M are available in a 4 mm × 4mm QFN. The exposed pad on the bottom of the package is sized differently between the two devices. The TPA4411RTJ PowerPAD is larger than the TPA4411MRTJ PowerPAD. Please see the layout and mechanical drawings at the end of the datasheet for proper sizing.

SGND and PGND Connections

The SGND and PGND pins of the TPA4411 and TPA4411M must be routed separately back to the decoupling capacitor in order to provide proper device operation. If the SGND and PGND pins are connected directly to each other, the part functions without risk of failure, but the noise and THD performance do not meet the specifications.

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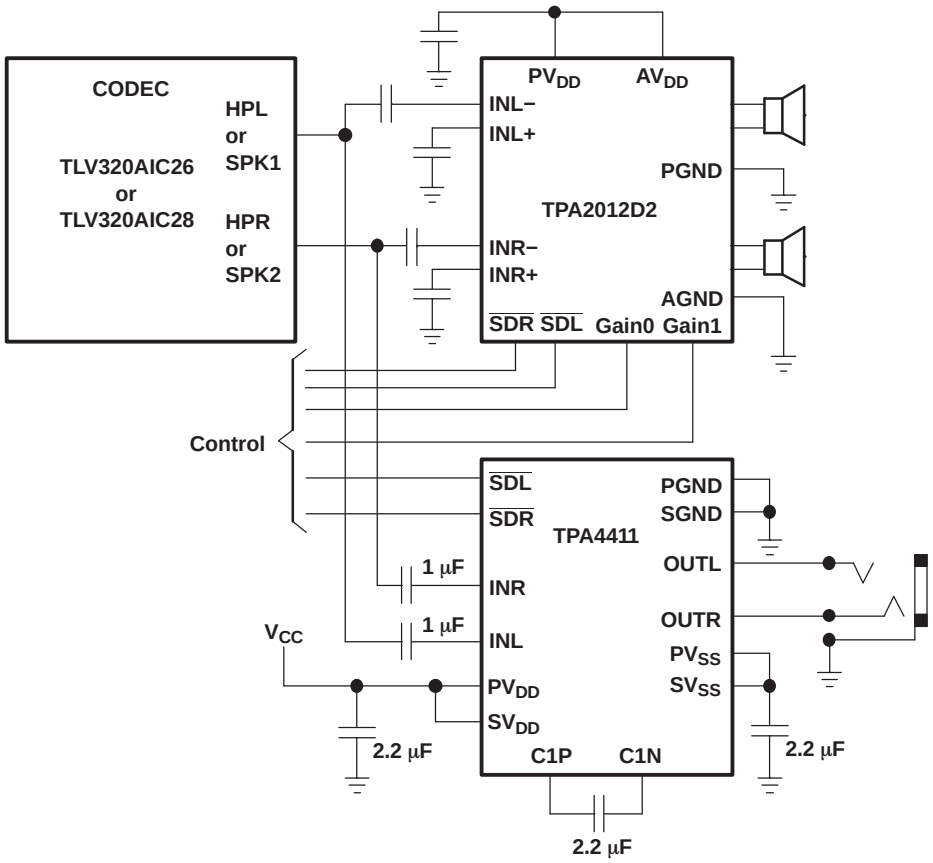
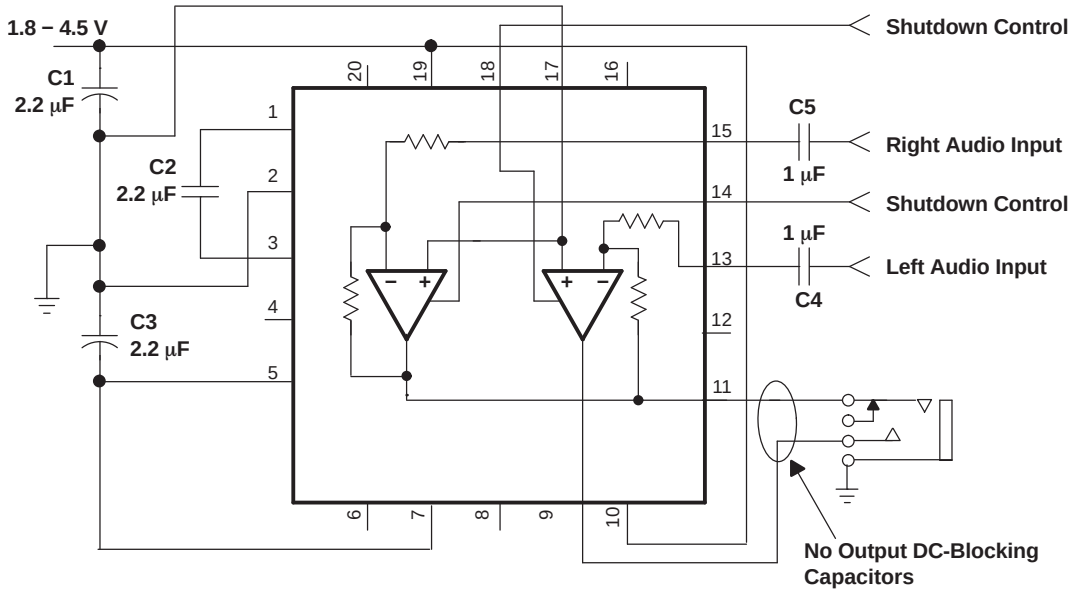


Figure 76. Application Circuit



Note: PowerPAD must be soldered down and plane must be floating.

Figure 77. Typical Circuit

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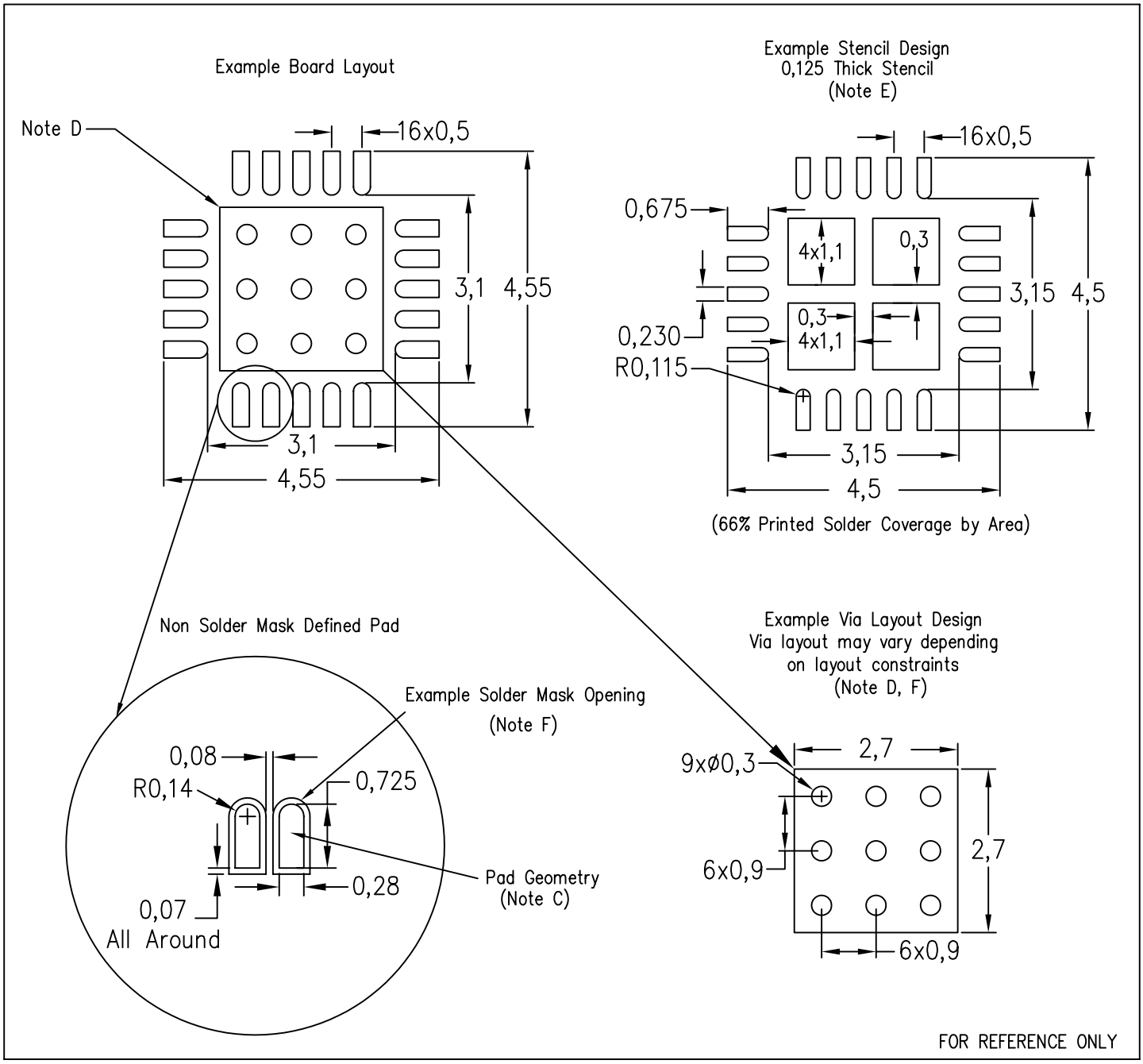
EXAMPLE LAND PATTERN

TPA4411RTJ

RTJ (S–PQFP–N20)

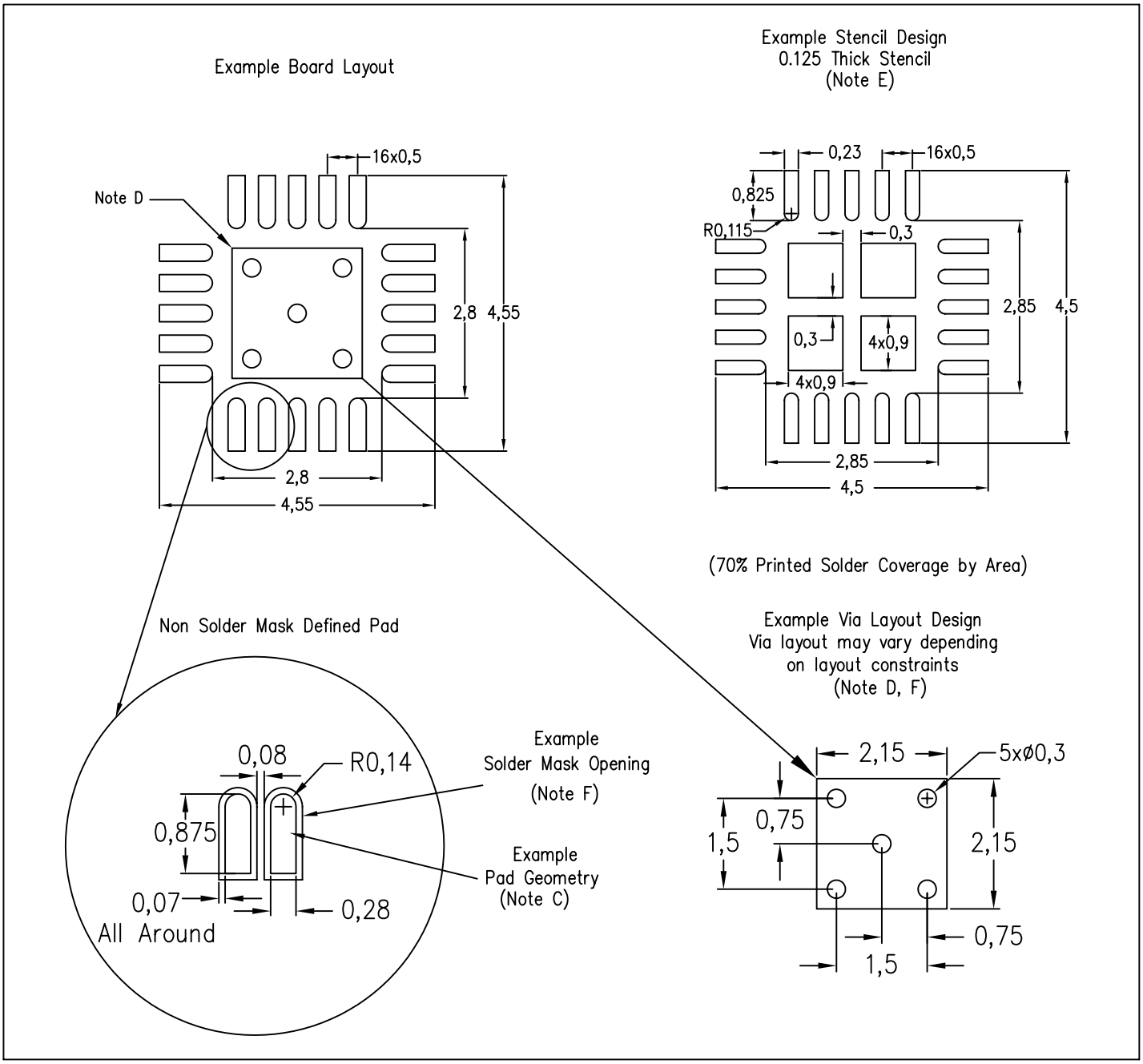


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–SM–782 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

EXAMPLE LAND PATTERN

TPA4411MRTJ

RTJ (S–PQFP–N20)



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPA4411MRTJR	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BPB	Samples
TPA4411MRTJRG4	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BPB	Samples
TPA4411MRTJT	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BPB	Samples
TPA4411MRTJTG4	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BPB	Samples
TPA4411RTJR	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AKQ	Samples
TPA4411RTJRG4	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AKQ	Samples
TPA4411RTJT	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AKQ	Samples
TPA4411RTJTG4	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AKQ	Samples
TPA4411YZHR	ACTIVE	DSBGA	YZH	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKT	Samples
TPA4411YZHT	ACTIVE	DSBGA	YZH	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

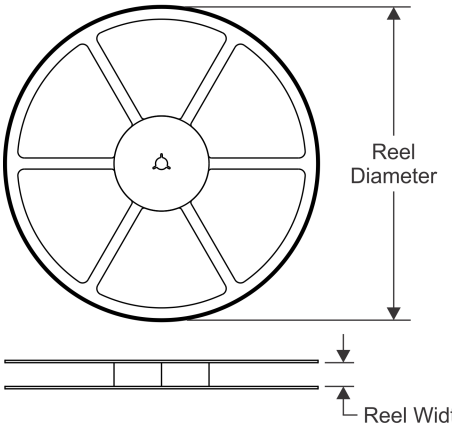
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

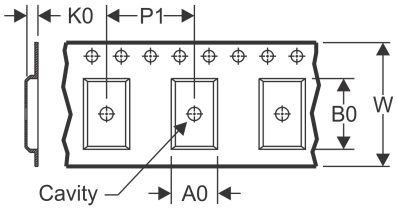
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

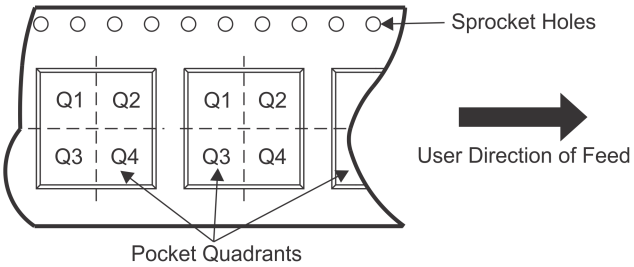


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

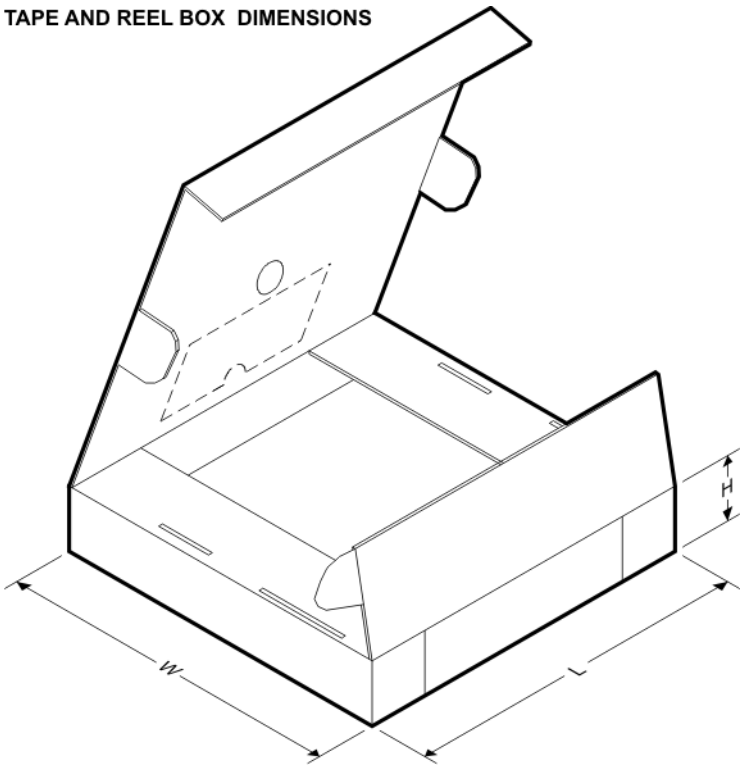
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA4411MRTJR	QFN	RTJ	20	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q1
TPA4411MRTJT	QFN	RTJ	20	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q1
TPA4411RTJR	QFN	RTJ	20	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPA4411RTJT	QFN	RTJ	20	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPA4411YZHR	DSBGA	YZH	16	3000	178.0	8.4	2.35	2.35	0.81	4.0	8.0	Q1
TPA4411YZHR	DSBGA	YZH	16	3000	180.0	8.4	2.35	2.35	0.81	4.0	8.0	Q1
TPA4411YZHT	DSBGA	YZH	16	250	178.0	8.4	2.35	2.35	0.81	4.0	8.0	Q1
TPA4411YZHT	DSBGA	YZH	16	250	180.0	8.4	2.35	2.35	0.81	4.0	8.0	Q1
TPA4411YZHT	DSBGA	YZH	16	250	180.0	8.4	2.38	2.4	0.8	4.0	8.0	Q1

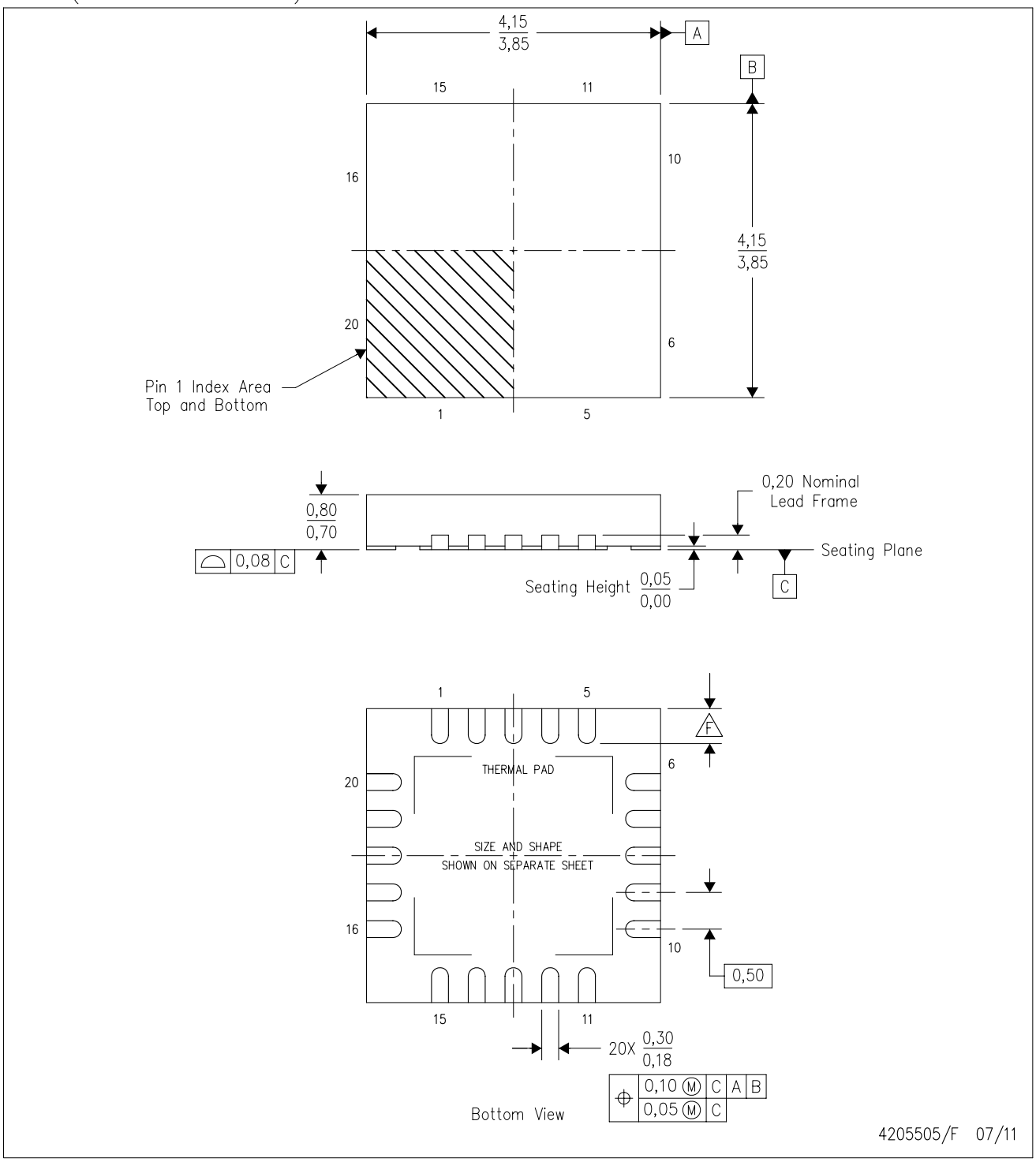
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA4411MRTJR	QFN	RTJ	20	3000	338.1	338.1	20.6
TPA4411MRTJT	QFN	RTJ	20	250	210.0	185.0	35.0
TPA4411RTJR	QFN	RTJ	20	3000	338.1	338.1	20.6
TPA4411RTJT	QFN	RTJ	20	250	210.0	185.0	35.0
TPA4411YZHR	DSBGA	YZH	16	3000	217.0	193.0	35.0
TPA4411YZHR	DSBGA	YZH	16	3000	220.0	220.0	34.0
TPA4411YZHT	DSBGA	YZH	16	250	217.0	193.0	35.0
TPA4411YZHT	DSBGA	YZH	16	250	220.0	220.0	34.0
TPA4411YZHT	DSBGA	YZH	16	250	210.0	185.0	35.0

RTJ (S-PWQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

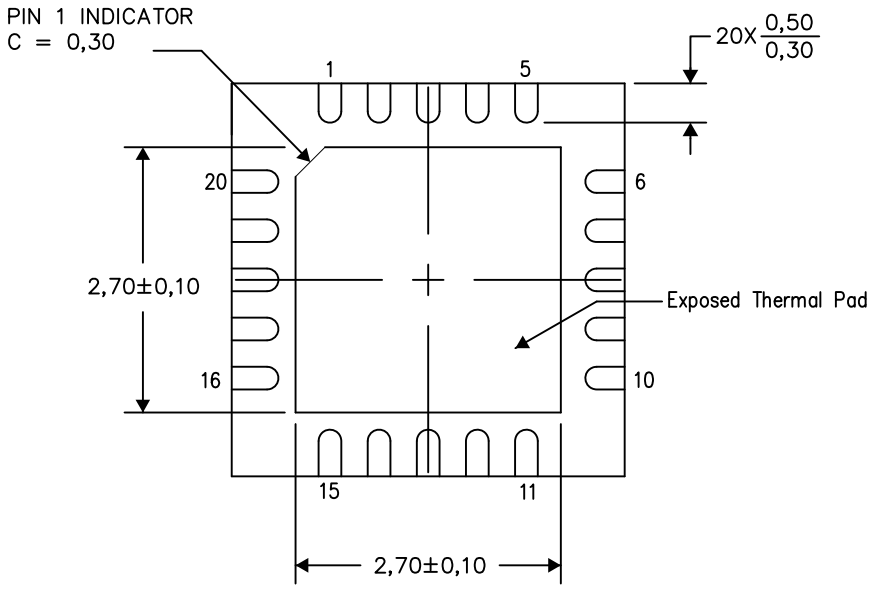
RTJ (S-PWQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



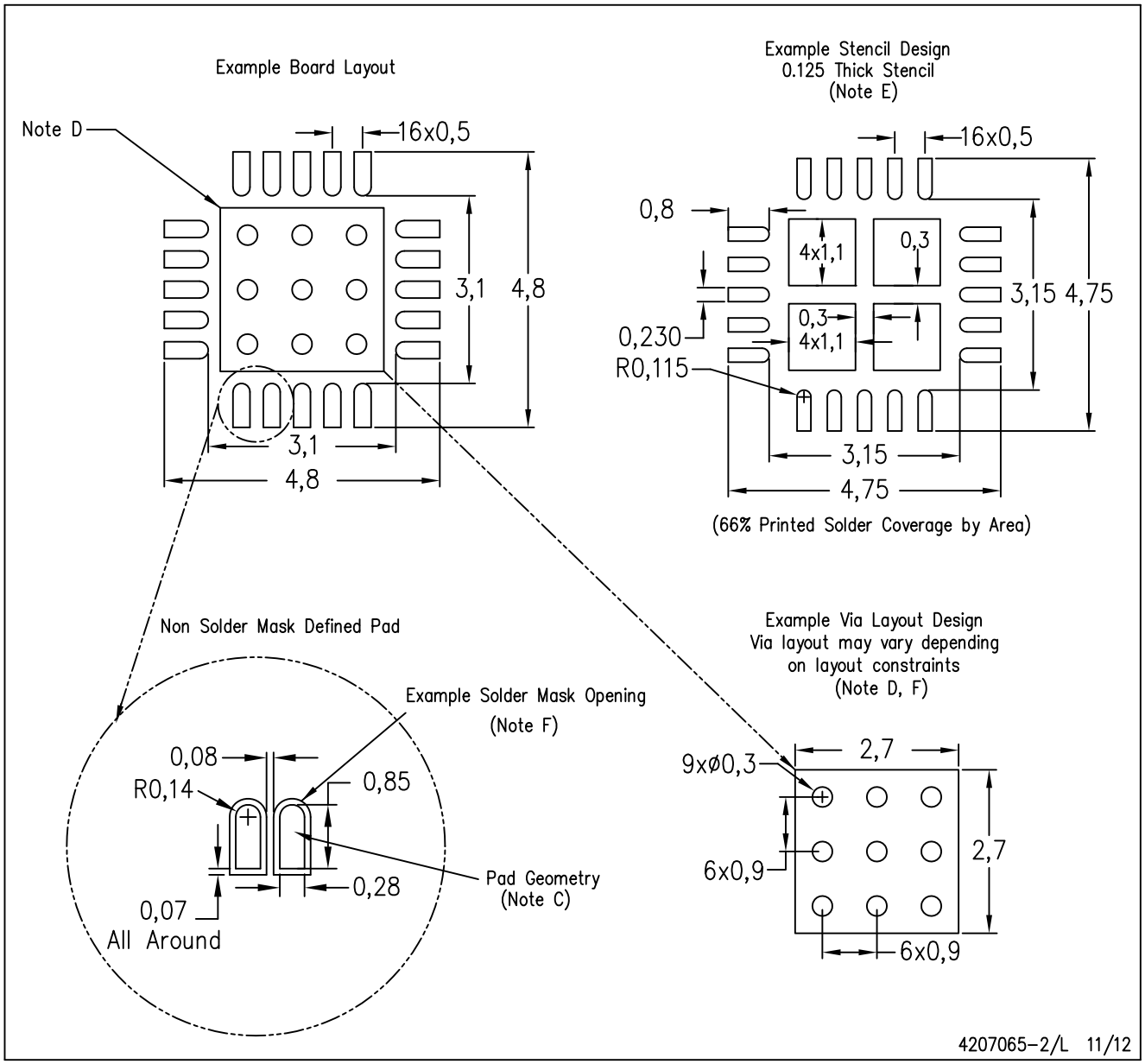
Bottom View

Exposed Thermal Pad Dimensions

4206256-2/R 11/12

NOTE: All linear dimensions are in millimeters

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RTJ (S-PWQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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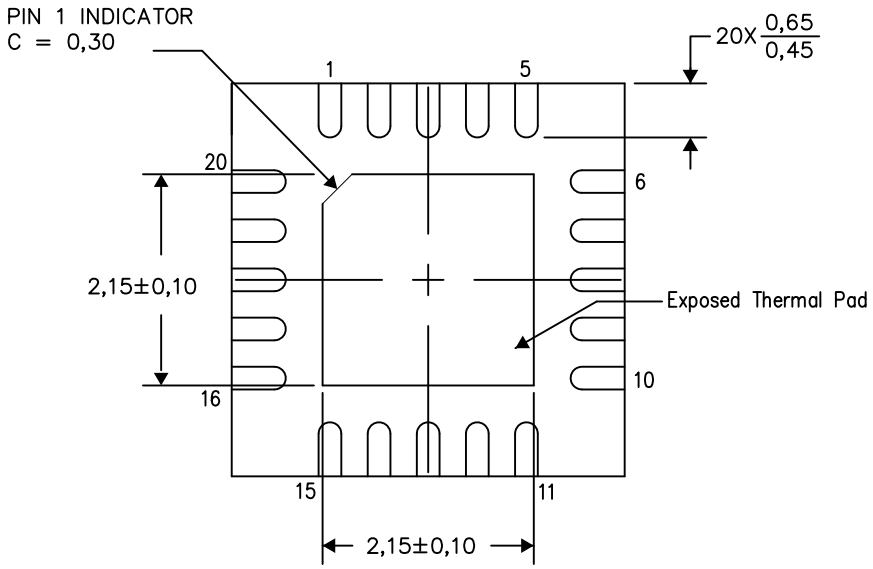


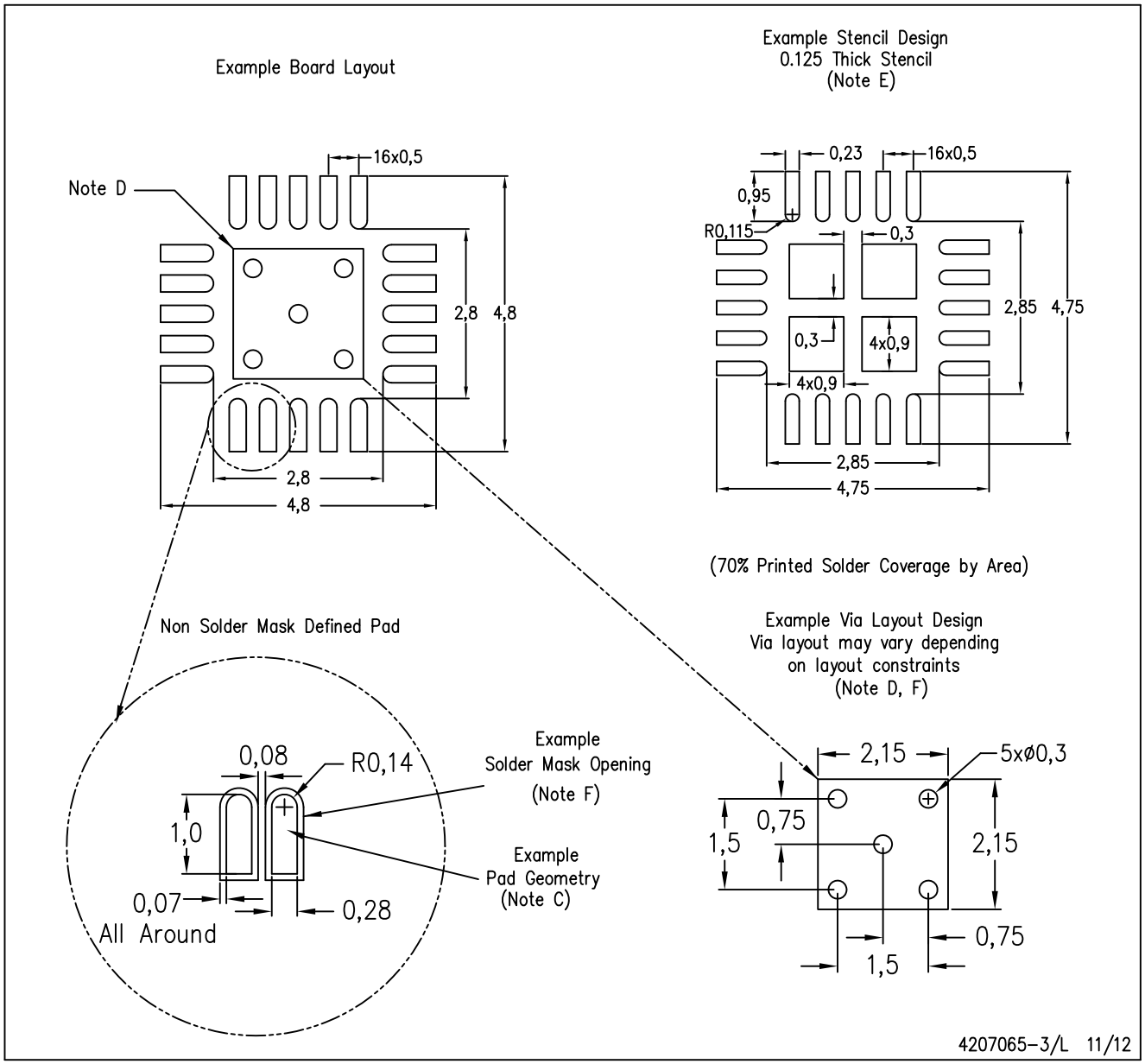
Bottom View

Exposed Thermal Pad Dimensions

4206256-3/R 11/12

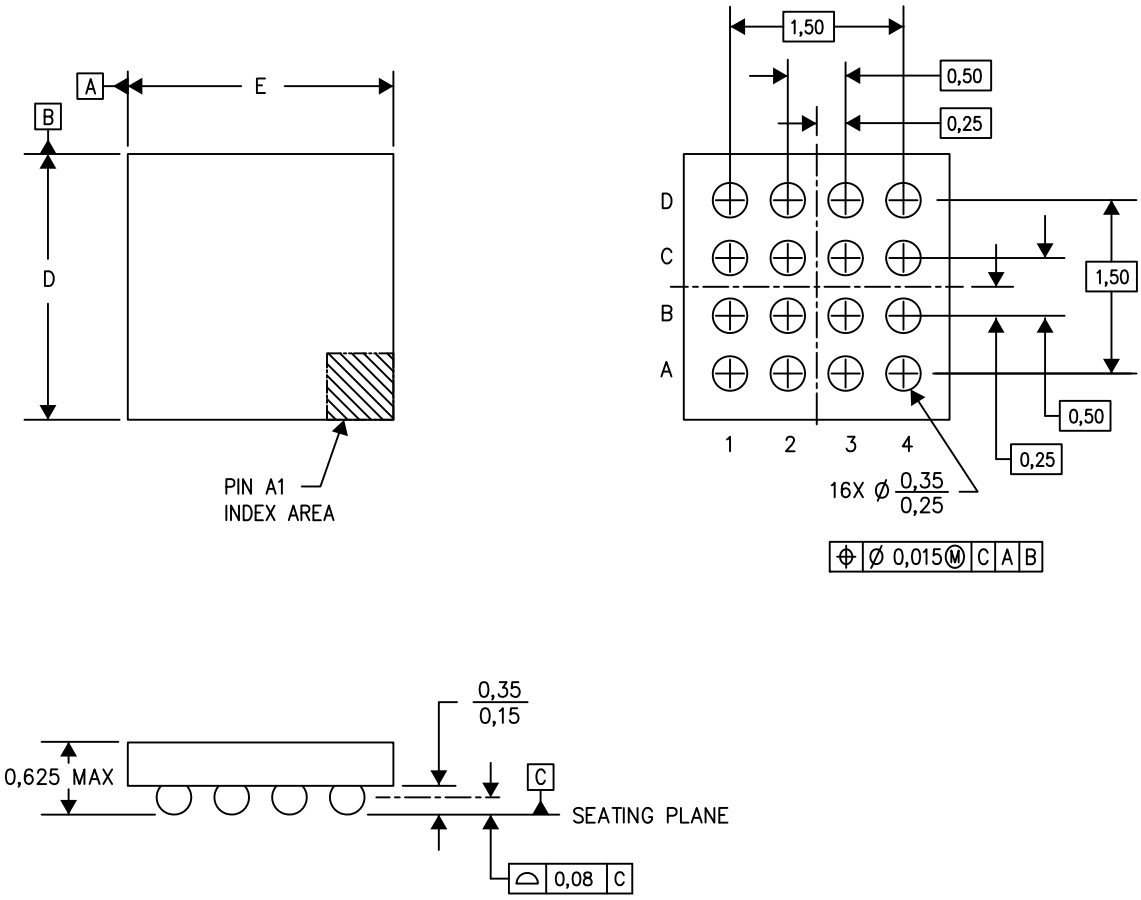
NOTE: All linear dimensions are in millimeters

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

YZH (S–XBGA–N16) DIE–SIZE BALL GRID ARRAY



D: Max = 2.196 mm, Min =2.136 mm

E: Max = 2.196 mm, Min =2.136 mm

4205060/F 05/13

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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