LM4924 Boomer™ Audio Power Amplifier Series 2 Cell Battery, 40mW Per Channel Output Capacitor-Less (OCL) Stereo Headphone Audio Amplifier

Check for Samples: LM4924

FEATURES

- **2-Cell 1.5V to 3.6V Battery Operation**
- **OCL Mode for Stereo Headphone Operation**
- **Unity-Gain Stable**
- **"Click and Pop" Suppression Circuitry for Shutdown On and Off Transients**
- **Active Low Micropower Shutdown**
- **Thermal Shutdown Protection Circuitry**

APPLICATIONS

- **Portable Two-Cell Audio Products**
- **Portable Two-Cell Electronic Devices**

KEY SPECIFICATIONS

- **OCL Output Power**
  - **(R_L = 16Ω, V_{DD} = 3.0V, THD+N = 1%), 40mW (Typ)**
- **Micropower Shutdown Current, 0.1µA (Typ)**
- **Supply Voltage Operating Range, 1.5V < V_{DD} < 3.6V**
- **PSRR 100Hz, V_{DD} = 3.0V, A_V = 2.5, 66dB (Typ)**

DESCRIPTION

The LM4924 is a Output Capacitor-Less (OCL) stereo headphone amplifier, which when connected to a 3.0V supply, delivers 40mW per channel to a 16Ω load with less than 1% THD+N.

With the LM4924 packaged in the VSSOP and SON packages, the customer benefits include low profile and small size. These packages minimizes PCB area and maximizes output power.

The LM4924 features circuitry that reduces output transients ("clicks" and "pops") during device turn-on and turn-off, and Mute On and Off. An externally controlled, low-power consumption, active-low shutdown mode is also included in the LM4924. Boomer audio power amplifiers are designed specifically to use few external components and provide high quality output power in a surface mount packages.

Typical Application

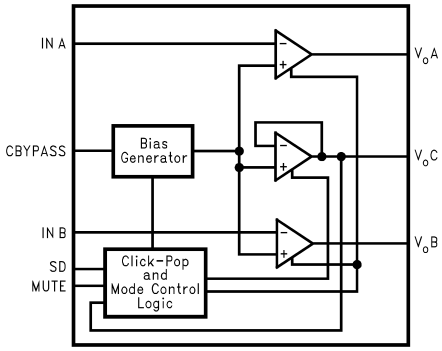

Figure 1. Block Diagram

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Connection Diagrams

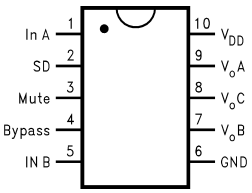

Figure 2. VSSOP Package
Top View
See Package Number DGS for VSSOP

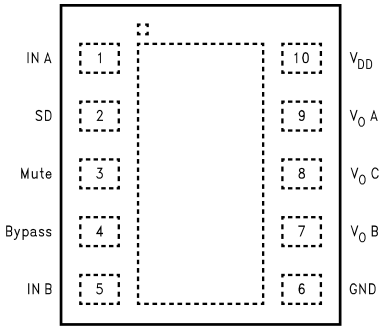

Figure 3. SON Package
Top View
See Package Number DSC0010A

Typical Connections

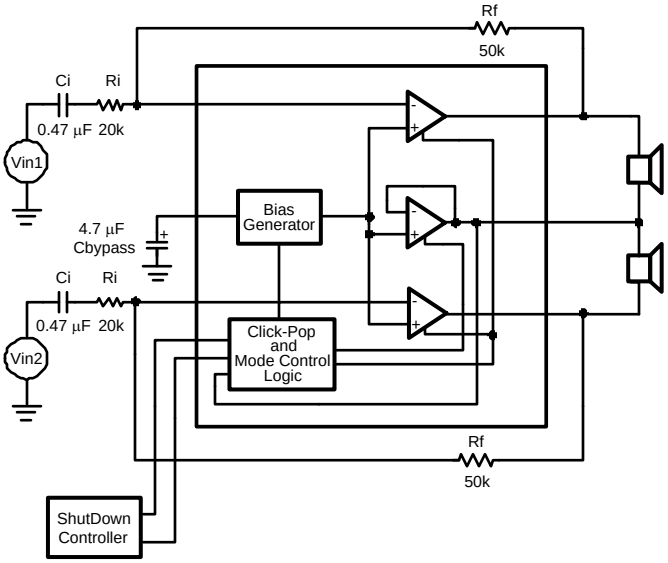

Figure 4. Typical OCL Output Configuration Circuit

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2]

Supply Voltage		3.8V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation[3]		Internally limited
ESD Susceptibility[4]		2000V
ESD Susceptibility on pin 7, 8, and 9[4]		2kV
ESD Susceptibility[5]		200V
Junction Temperature		150°C
Solder Information	Small Outline Package Vapor Phase (60sec)	215°C
	Infrared (15 sec)	220°C
Thermal Resistance	θ_{JA} (typ) DGS	175°C/W
	θ_{JA} (typ) DSC0010A	73°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensue specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments' Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A and must be derated at elevated temperatures. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. For the LM4924, T_{JMAX} = 150°C. For the θ_{JA}s, please see the Application Information section or the Absolute Maximum Ratings section.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine model, 220pF–240pF discharged through all pins.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ +85°C
	Supply Voltage	1.5V ≤ V_{DD} ≤ 3.6V

Electrical Characteristics V_{DD} = 3.0V[1][2]

The following specifications apply for the circuit shown in Figure 4, unless otherwise specified. A_V = 2.5, R_L = 16Ω. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4924		Units (Limits)
			Typical[3]	Limit[4]	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, R_L = ∞[5]	1.5	1.9	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	1	µA (max)
V_{OS}	Output Offset Voltage		1	10	mV (max)
P_O	Output Power[6]	f = 1kHz, per channel			
		OCL (Figure 4), THD+N = 1%	40	30	mW (min)
V_{NO}	Output Voltage Noise	20Hz to 20kHz, A-weighted, Figure 4	13		μV_{RMS}
THD		P_O = 10mW	0.1	0.5	%
Crosstalk		Freq = 1kHz	45	35	dB (min)
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P} sine wave			
		Freq = 100Hz, OCL	66	58	dB (min)
$T_{WAKE-UP}$	Wake-Up Time	1.5V ≤ V_{DD} ≤ 3.6V, Figure 4	230		msec

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(2) All voltages are measured with respect to the ground (GND) pins unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(5) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.
(6) Output power is measured at the device terminals.

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Electrical Characteristics V_{DD} = 3.0V(1)(2) (continued)

The following specifications apply for the circuit shown in Figure 4, unless otherwise specified. A_V = 2.5, R_L = 16Ω. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4924		Units (Limits)
			Typical(3)	Limit(4)	
V_{IH}	Control Logic High	1.5V ≤ V_{DD} ≤ 3.6V		0.7V_{DD}	V (min)
V_{IL}	Control Logic Low	1.5V ≤ V_{DD} ≤ 3.6V		0.3V_{DD}	V (max)
Mute Attenuation		1V_{PP} Reference, R_{IN} = 20k, R_{FB} = 50k	90	70	dB

Electrical Characteristics V_{DD} = 1.8V(1)(2)

The following specifications apply for the circuit shown in Figure 4, unless otherwise specified. A_V = 2.5, R_L = 16Ω. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4924		Units (Limits)
			Typical(3)	Limit(4)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, R_L = ∞ (5)	1.4		mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1		µA (max)
V_{OS}	Output Offset Voltage		1		mV (max)
P_O	Output Power (6)	f = 1kHz			
		OCL Per channel, Figure 4, Freq = 1kHz THD+N = 1%	10		mW
V_{NO}	Output Voltage Noise	20Hz to 20kHz, A-weighted, Figure 4	10		µV_{RMS}
THD		P_O = 5mW	0.1		%
Crosstalk		Freq = 1kHz	45		dB (min)
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P} sine wave			
		Freq = 100Hz, OCL	66		dB

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensue specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
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(5) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.
(6) Output power is measured at the device terminals.

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Typical Performance Characteristics

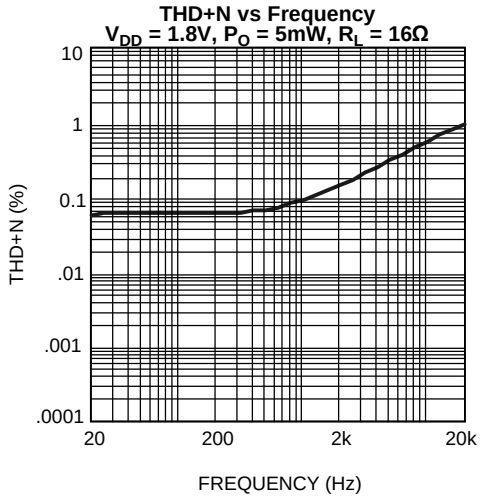

Figure 5.

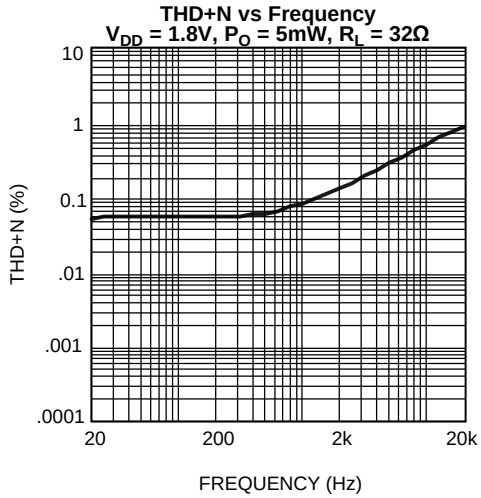

Figure 6.

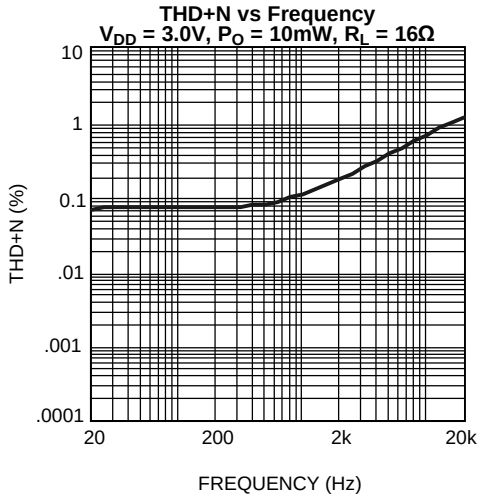

Figure 7.

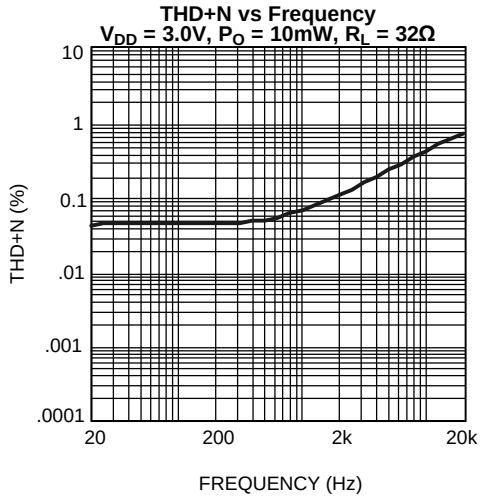

Figure 8.

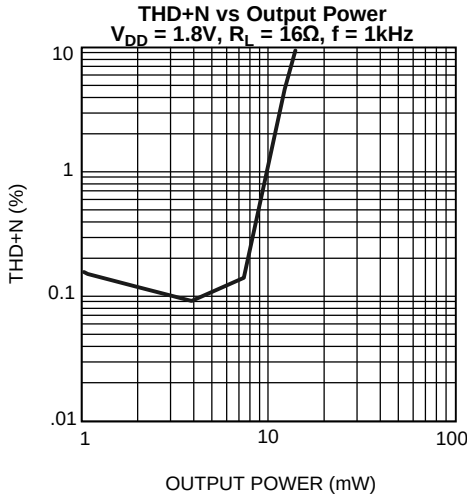

Figure 9.

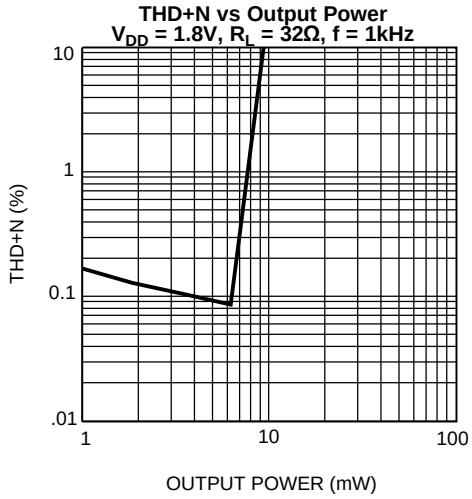

Figure 10.

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Typical Performance Characteristics (continued)

THD+N vs Output Power
V_{DD} = 3.0V, R_L = 16Ω, f = 1kHz

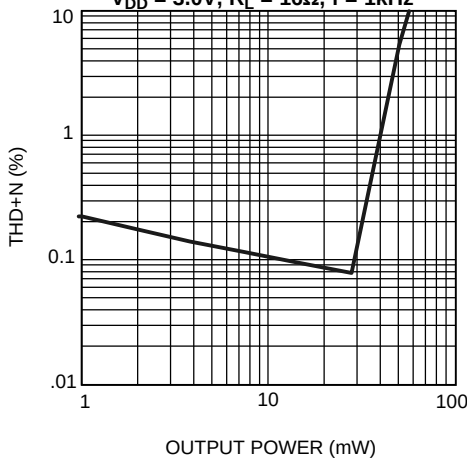

Figure 11.

THD+N vs Output Power
V_{DD} = 3.0V, R_L = 32Ω, f = 1kHz

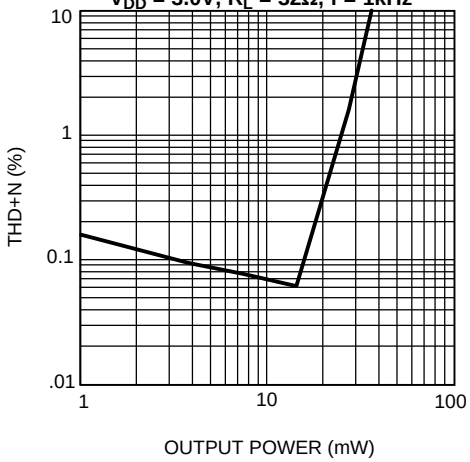

Figure 12.

Power Supply Rejection Ratio
V_{DD} = 1.8V, R_L = 16Ω,
Vripple = 200mVp-p, Input Terminated into 10Ω load

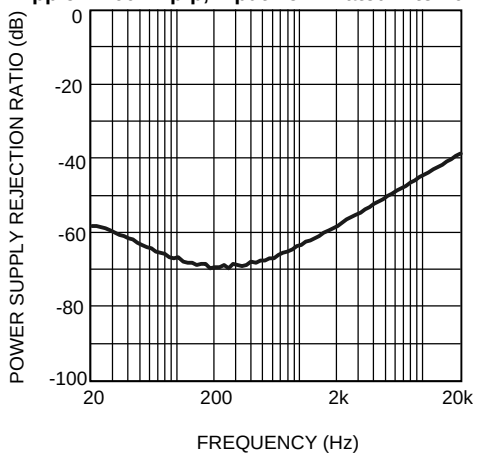

Figure 13.

Power Supply Rejection Ratio
V_{DD} = 3.0V, R_L = 16Ω,
Vripple = 200mVp-p, Input Terminated into 10Ω load

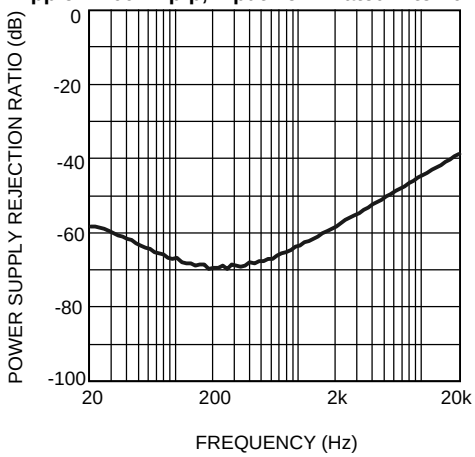

Figure 14.

Noise Floor
V_{DD} = 1.8V, R_L = 16Ω

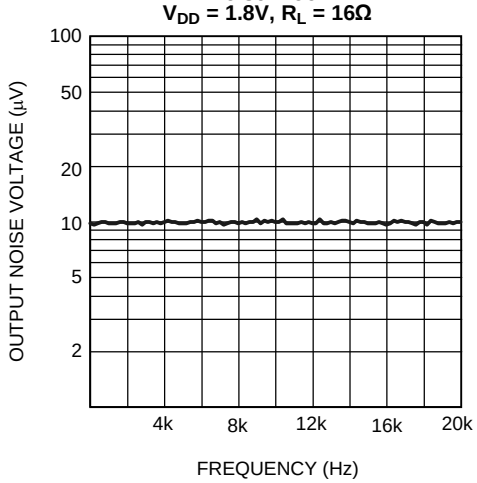

Figure 15.

Noise Floor
V_{DD} = 3.0V, R_L = 16Ω

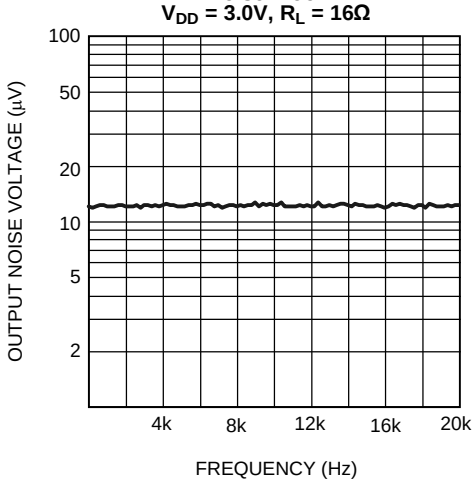

Figure 16.

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Typical Performance Characteristics (continued)

Channel Separation
R_L = 16Ω

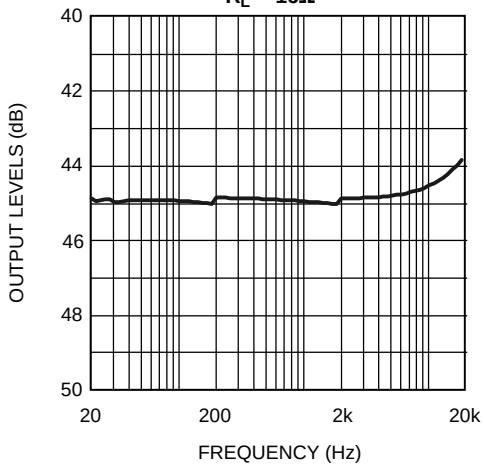

Figure 17.

Output Power vs Load Resistance
f = 1kHz. from top to bottom:
V_{DD} = 3.0V, 10%THD+N; V_{DD} = 3.0V, 1%THD+N
V_{DD} = 1.8V, 10%THD+N; V_{DD} = 1.8V, 1%THD+N

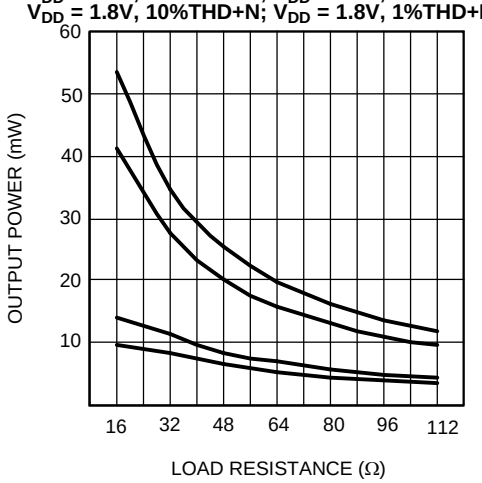

Figure 18.

Output Power
vs
Supply Voltage
R_L = 16Ω, from top to bottom:
THD+N = 10%; THD+N = 1%

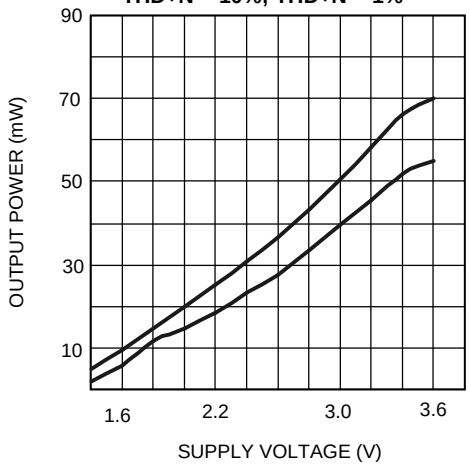

Figure 19.

Output Power vs Supply Voltage
R_L = 32Ω, from top to bottom:
THD+N = 10%; THD+N = 1%

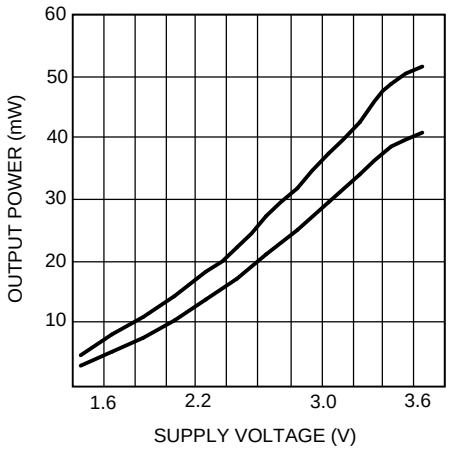

Figure 20.

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Typical Performance Characteristics (continued)

Power Dissipation vs Output Power
V_{DD} = 1.8V, f = 1kHz, from top to bottom:
R_L = 16Ω; R_L = 32Ω

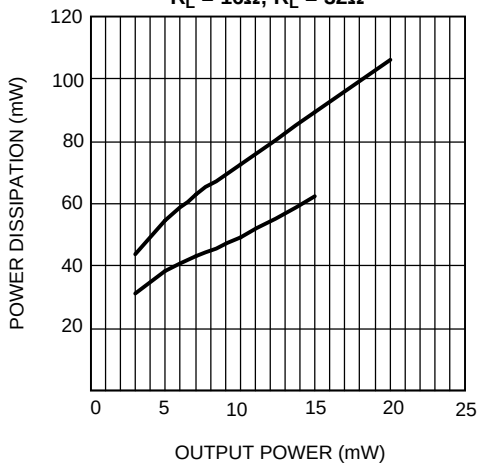

Figure 21.

Power Dissipation vs Output Power
V_{DD} = 3.0V, f = 1kHz, from top to bottom:
R_L = 16Ω; R_L = 32Ω

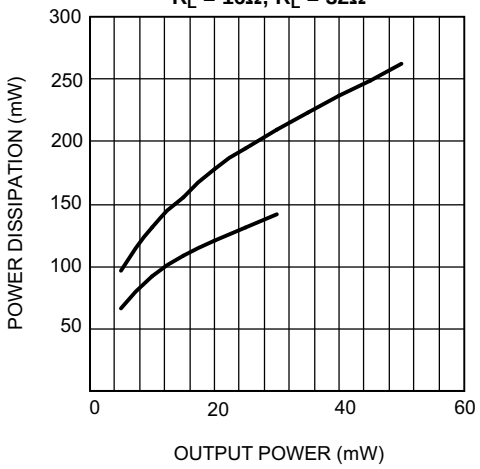

Figure 22.

Supply Current vs Supply Voltage

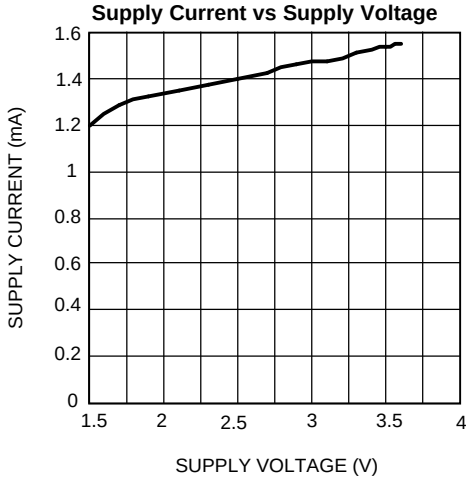

Figure 23.

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Application Information

ELIMINATING OUTPUT COUPLING CAPACITORS

Typical single-supply audio amplifiers that drive single-ended (SE) headphones use a coupling capacitor on each SE output. This output coupling capacitor blocks the half-supply voltage to which the output amplifiers are typically biased and couples the audio signal to the headphones. The signal return to circuit ground is through the headphone jack's sleeve.

The LM4924 eliminates these output coupling capacitors. V_oC is internally configured to apply a $1/2V_{DD}$ bias voltage to a stereo headphone jack's sleeve. This voltage matches the quiescent voltage present on the V_oA and V_oB outputs that drive the headphones. The headphones operate in a manner similar to a bridge-tied-load (BTL). The same DC voltage is applied to both headphone speaker terminals. This results in no net DC current flow through the speaker. AC current flows through a headphone speaker as an audio signal's output amplitude increases on the speaker's terminal.

The headphone jack's sleeve is not connected to circuit ground. Using the headphone output jack as a line-level output will place the LM4924's bandgap $1/2V_{DD}$ bias on a plug's sleeve connection. This presents no difficulty when the external equipment uses capacitively coupled inputs. For the very small minority of equipment that is DC-coupled, the LM4924 monitors the current supplied by the amplifier that drives the headphone jack's sleeve. If this current exceeds $500mA_{PK}$, the amplifier is shutdown, protecting the LM4924 and the external equipment.

BYPASS CAPACITOR VALUE SELECTION

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_{BYPASS}, the capacitor connected to the BYPASS pin. Since C_{BYPASS} determines how fast the LM4924 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4924's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 4.7µF along with a small value of C_i (in the range of 0.1µF to 0.47µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops. This ensures that output transients are eliminated when power is first applied or the LM4924 resumes operation after shutdown.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4924 contains circuitry that eliminates turn-on and shutdown transients ("clicks and pops"). For this discussion, turn-on refers to either applying the power supply voltage or when the micro-power shutdown mode is deactivated.

As the $V_{DD}/2$ voltage present at the BYPASS pin ramps to its final value, the LM4924's internal amplifiers are configured as unity gain buffers. An internal current source charges the capacitor connected between the BYPASS pin and GND in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches $V_{DD}/2$. As soon as the voltage on the bypass pin is stable, the device becomes fully operational and the amplifier outputs are reconnected to their respective output pins. Although the BYPASS pin current cannot be modified, changing the size of C_{BYPASS} alters the device's turn-on time. There is a linear relationship between the size of C_{BYPASS} and the turn-on time. Here are some typical turn-on times for various values of C_{BYPASS}.

AMPLIFIER CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4924 has three operational amplifiers internally. Two of the amplifier's have externally configurable gain while the other amplifier is internally fixed at the bias point acting as a unity-gain buffer. The closed-loop gain of the two configurable amplifiers is set by selecting the ratio of R_f to R_i. Consequently, the gain for each channel of the IC is

$$A_V = -(R_f/R_i) \quad (1)$$

By driving the loads through outputs V_{O1} and V_{O2} with V_{O3} acting as a buffered bias voltage the LM4924 does not require output coupling capacitors. The typical single-ended amplifier configuration where one side of the load is connected to ground requires large, expensive output coupling capacitors.

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A configuration such as the one used in the LM4924 has a major advantage over single supply, single-ended amplifiers. Since the outputs V_{O1}, V_{O2}, and V_{O3} are all biased at 1/2 V_{DD}, no net DC voltage exists across each load. This eliminates the need for output coupling capacitors that are required in a single-supply, single-ended amplifier configuration. Without output coupling capacitors in a typical single-supply, single-ended amplifier, the bias voltage is placed across the load resulting in both increased internal IC power dissipation and possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 2

$$P_{DMAX} = 4(V_{DD})^2 / (\pi^2 R_L) \quad (2)$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. Since the typical application is for headphone operation (16Ω impedance) using a 3.3V supply the maximum power dissipation is only 138mW. Therefore, power dissipation is not a major concern.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is important for low noise performance and high power supply rejection. The capacitor location on the power supply pins should be as close to the device as possible.

Typical applications employ a 3.0V regulator with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4924. A bypass capacitor value in the range of 0.1µF to 1µF is recommended for C_S.

MICRO POWER SHUTDOWN

The voltage applied to the $\overline{\text{SHUTDOWN}}$ pin controls the LM4924's shutdown function. Activate micro-power shutdown by applying a logic-low voltage to the $\overline{\text{SHUTDOWN}}$ pin. When active, the LM4924's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The trigger point is 0.4V (max) for a logic-low level, and 1.5V (min) for a logic-high level. The low 0.1µA (typ) shutdown current is achieved by applying a voltage that is as near as ground as possible to the $\overline{\text{SHUTDOWN}}$ pin. A voltage that is higher than ground may increase the shutdown current.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100kΩ pull-up resistor between the $\overline{\text{SHUTDOWN}}$ pin and V_{DD}. Connect the switch between the $\overline{\text{SHUTDOWN}}$ pin and ground. Select normal amplifier operation by opening the switch. Closing the switch connects the $\overline{\text{SHUTDOWN}}$ pin to ground, activating micro-power shutdown. The switch and resistor ensure that the $\overline{\text{SHUTDOWN}}$ pin will not float. This prevents unwanted state changes. In a system with a microprocessor or microcontroller, use a digital output to apply the control voltage to the $\overline{\text{SHUTDOWN}}$ pin. Driving the $\overline{\text{SHUTDOWN}}$ pin with active circuitry eliminates the pull-up resistor.

SELECTING EXTERNAL COMPONENTS

Selecting proper external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4924 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4924 is unity-gain stable which gives the designer maximum system flexibility. The LM4924 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than $1V_{rms}$ are available from sources such as audio codecs. Very large values should not be used for the gain-setting resistors. Values for R_i and R_f should be less than 1MΩ. Please refer to the section, AUDIO POWER AMPLIFIER DESIGN, for a more complete explanation of proper gain selection

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response and turn-on time.

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SELECTION OF INPUT CAPACITOR SIZE

Amplifiying the lowest audio frequencies requires a high value input coupling capacitor, C_i. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the headphones used in portable systems have little ability to reproduce signals below 60Hz. Applications using headphones with this limited frequency response reap little improvement by using a high value input capacitor.

In addition to system cost and size, turn-on time is affected by the size of the input coupling capacitor Ci. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage. This charge comes from the output via the feedback Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on time can be minimized. A small value of Ci (in the range of 0.1µF to 0.39µF), is recommended.

USING EXTERNAL POWERED SPEAKERS

The LM4924 is designed specifically for headphone operation. Often the headphone output of a device will be used to drive external powered speakers. The LM4924 has a differential output to eliminate the output coupling capacitors. The result is a headphone jack sleeve that is connected to V_{O3} instead of GND. For powered speakers that are designed to have single-ended signals at the input, the click and pop circuitry will not be able to eliminate the turn-on/turn-off click and pop. Unless the inputs to the powered speakers are fully differential the turn-on/turn-off click and pop will be very large.

AUDIO POWER AMPLIFIER DESIGN

A 30mW/32Ω Audio Amplifier

Given:	
Power Output	30mWrms
Load Impedance	32Ω
Input Level	1Vrms
Input Impedance	20kΩ

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the Typical Performance Characteristics section, the supply rail can be easily found.

Since 3.3V is a standard supply voltage in most applications, it is chosen for the supply rail in this example. Extra supply voltage creates headroom that allows the LM4924 to reproduce peaks in excess of 30mW without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does no violate the conditions explained in the POWER DISSIPATION section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 3.

$$A_V \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (3)$$

From Equation 3, the minimum A_V is 0.98; use A_V = 1. Since the desired input impedance is 20kΩ, and with A_V equal to 1, a ratio of 1:1 results from Equation 1 for R_f to R_i. The values are chosen with R_i = 20kΩ and R_f = 20kΩ.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz \quad (4)$$

and an

$$f_H = 20kHz \times 5 = 100kHz \quad (5)$$

As mentioned in the SELECTING EXTERNAL COMPONENTS section, R_i and C_i create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation 4.

$$C_i \geq 1/(2\pi R_i f_L) \quad (6)$$

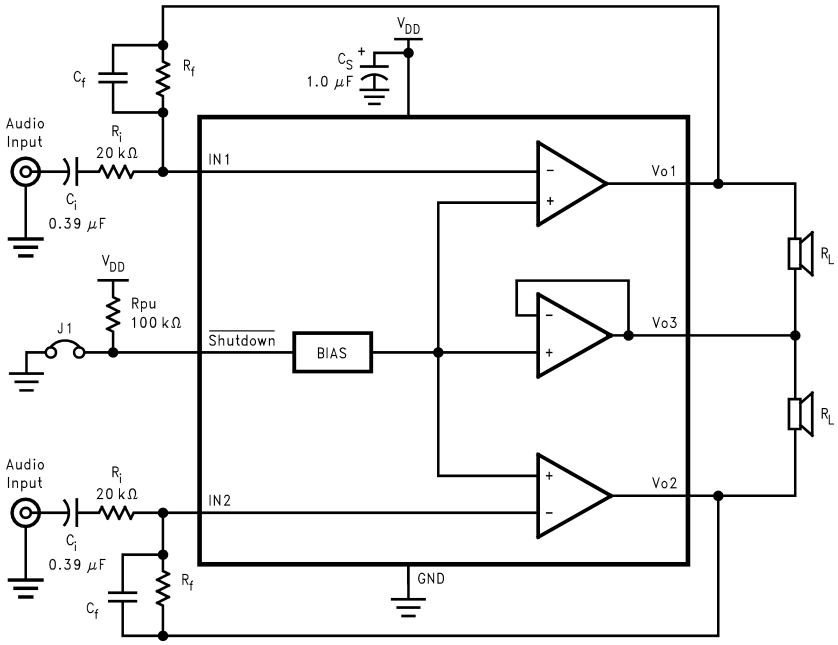
The result is

$$1/(2\pi*20k\Omega*20Hz) = 0.397\mu F \quad (7)$$

Use a 0.39µF capacitor, the closest standard value.

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_V. With an A_V = 1 and f_H = 100kHz, the resulting GBWP = 100kHz which is much smaller than the LM4924 GBWP of 11MHz. This figure displays that if a designer has a need to design an amplifier with higher differential gain, the LM4924 can still be used without running into bandwidth limitations.

HIGHER GAIN AUDIO AMPLIFIER



The LM4924 is unity-gain stable and requires no external components besides gain-setting resistors, input coupling capacitors, and proper supply bypassing in the typical application. However, if a very large closed-loop differential gain is required, a feedback capacitor (C_f) may be needed to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R_f and C_f will cause frequency response roll off before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency roll off is Rf = 20kΩ and C_f = 25pF. These components result in a -3dB point of approximately 320kHz.

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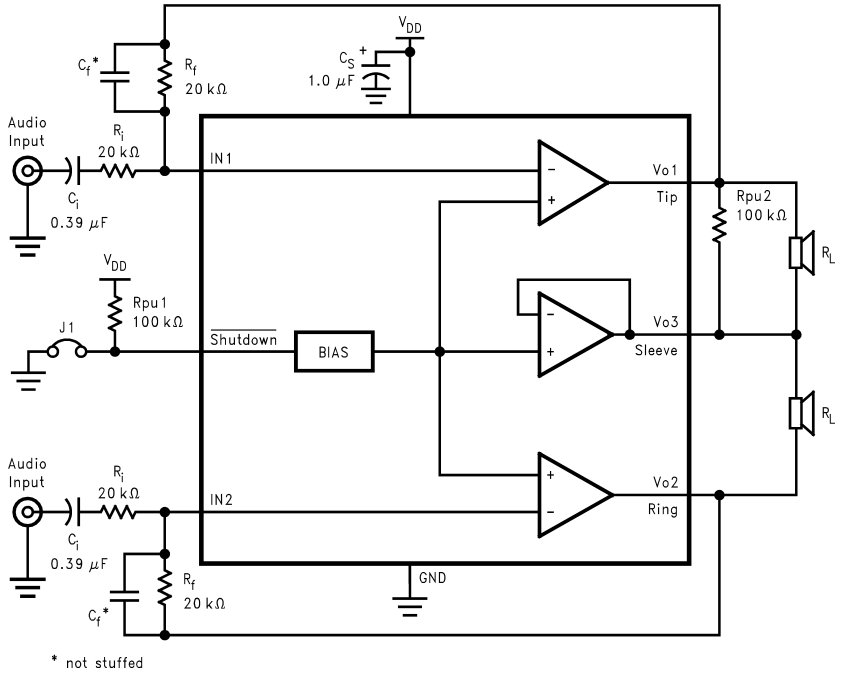
REFERENCE DESIGN BOARD and LAYOUT GUIDELINES VSSOP & SON BOARDS



A. $R_{PU}2$ is not required. It is used for test measurement purposes only.

PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

Minimization of THD

PCB trace impedance on the power, ground, and all output traces should be minimized to achieve optimal THD performance. Therefore, use PCB traces that are as wide as possible for these connections. As the gain of the amplifier is increased, the trace impedance will have an ever increasing adverse affect on THD performance. At unity-gain (0dB) the parasitic trace impedance effect on THD performance is reduced but still a negative factor in the THD performance of the LM4924 in a given application.

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GENERAL MIXED SIGNAL LAYOUT RECOMMENDATION

Power and Ground Circuits

For two layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can greatly enhance low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will require a greater amount of design time but will not increase the final price of the board. The only extra parts required may be some jumpers.

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "PI-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. Further, place digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

Placement of Digital and Analog Components

All digital components and high-speed digital signal traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

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REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4924MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	GB7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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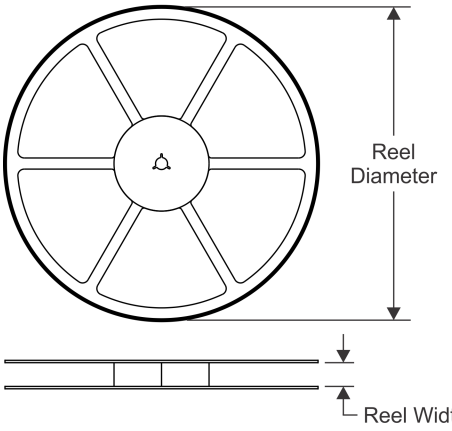
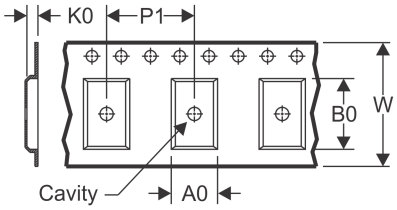
TAPE AND REEL INFORMATION

REEL DIMENSIONS

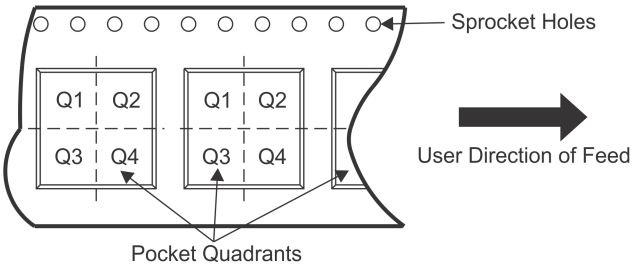


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

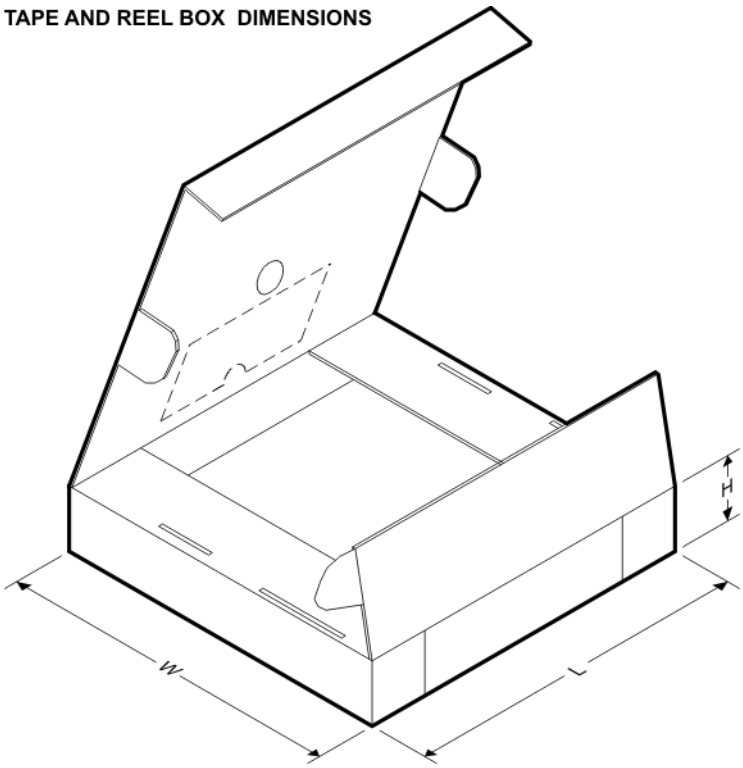
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4924MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

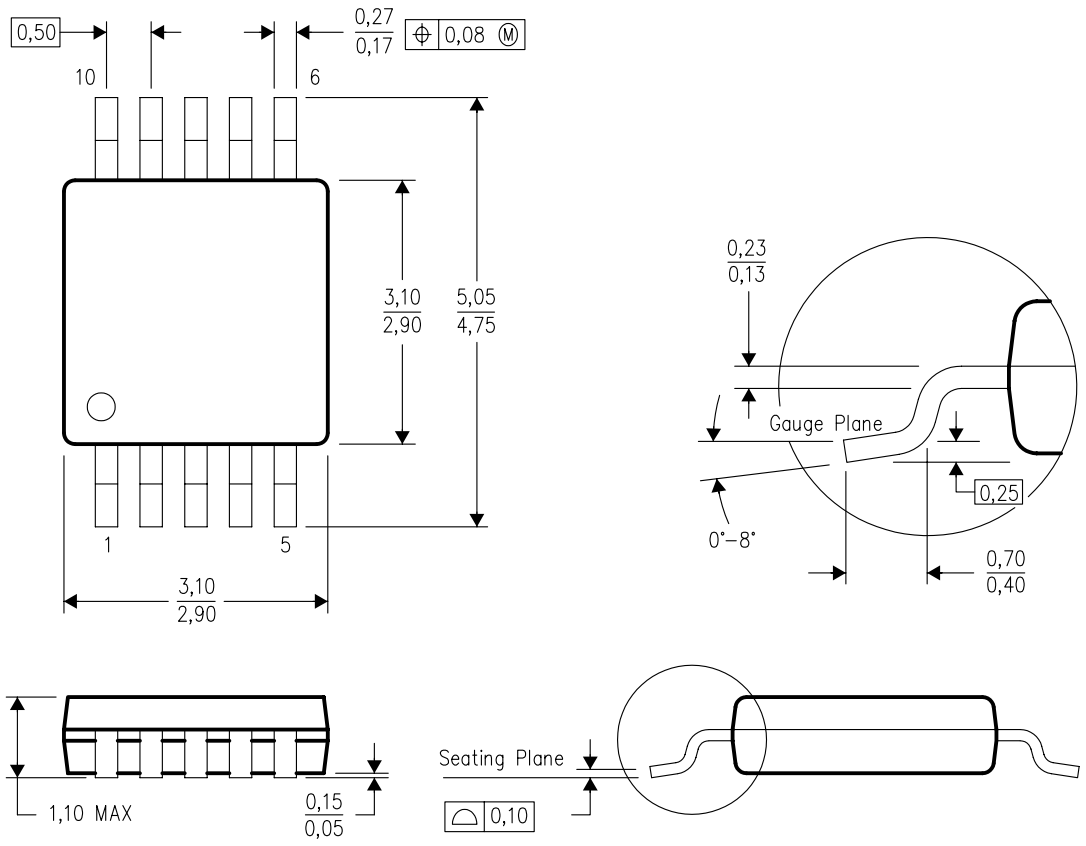
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4924MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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