LM4921 Boomer® Audio Power Amplifier Series Low Voltage I²S 16-Bit Stereo DAC with Stereo Headphone Power Amplifiers and Volume Control

Check for Samples: LM4921

FEATURES

- **16-Bit Resolution Stereo DAC**
- **I^2S Digital Audio Data Serial Interface**
- **SPI Serial Interface (Control Register)**
- **Volume Control (32 steps; 1.5 dB Increments)**
- **Up to 50mW/Channel Stereo Headphone Amplifier**
- **Zero Crossing Detection for Silent Attenuation Steps**
- **$2.6V_{DC}$ to $5.0V_{DC}$ Digital Supply Voltage Range**
- **$2.6V_{DC}$ to $5.5V_{DC}$ Analog Supply Voltage Range (See (1))**
- **Unity-Gain Stable Headphone Amplifiers**
- **Available in the 20-bump DSBGA Package**

KEY SPECIFICATIONS

- **PSRR at 217Hz, A/DV_{DD} = 3V, (See Figure 1): 52dB (typ)**
- **P_{OUT} at AV_{DD} = 3.0V, 32Ω**
  - **< 0.05% THD: 13mW (typ)**
  - **< 0.05% THD: 26mW (typ)**
- **Supply Voltage Range**
  - **DV_{DD}: 2,6V to 5.0V**
  - **AV_{DD}: (See (1)) 2.6V to 5.5V**
- **Shutdown Current: 1μA (typ)**

(1) Best operation is achieved by maintaining $3.0V \le AV_{DD} \le 5.0V$ and $3.0V \le DV_{DD} \le 5.0V$.

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Portable Electronic Devices**

DESCRIPTION

The LM4921 combines a 16-bit resolution stereo I^2S input digital-to-analog converter (DAC) with a stereo headphone audio power amplifier. It is primarily designed for demanding applications in mobile phones and other portable communication device applications. The LM4921 features an I^2S serial interface for the digital audio information and a 16-bit SPI serial interface for internal register control and communication. With AV_{DD} and DV_{DD} = $3.0V_{DC}$ and driving a 32Ω single-ended load to a $26mW_{RMS}$ output level the distortion (THD+N) of the LM4921 will be less than 0.5%. The LM4921 also features a programmable 32-step digital volume control accessed through an SPI interface.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. It is, therefore, ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4921 features a low-power consumption shutdown mode, and also has an internal thermal shutdown protection mechanism.

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Typical Application

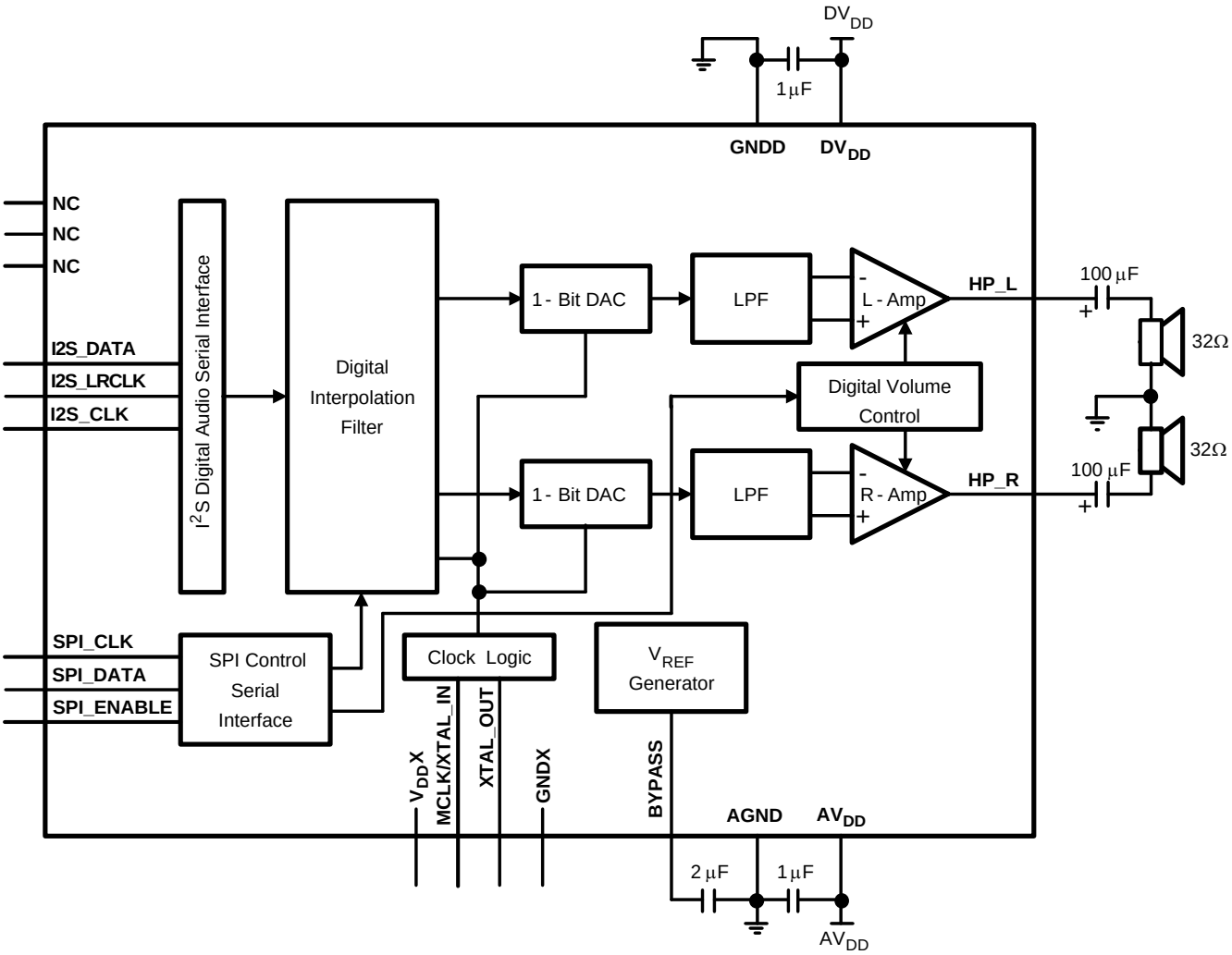

Figure 1. Typical Audio Amplifier Application Circuit

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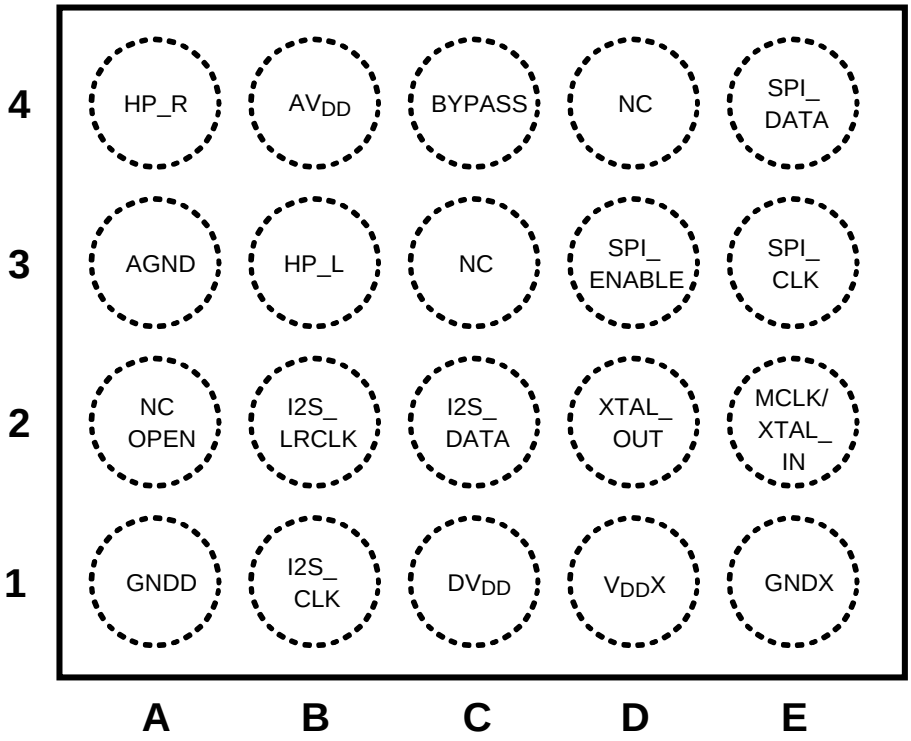
Connection Diagrams



(1) NC - No Connection

Figure 2. LM4921 20-Bump DSBGA Pin Configuration – Top View
See Package Number YZR0020

LM4921 I/O PIN DESCRIPTIONS

PIN # (ITL)	PIN NAME	PIN TYPE Input-I, Output-O, Power-P, No Connect-NC	PIN DESCRIPTION
B1	I2S_CLK	I/O	I2S Clock
C2	I2S_DATA	I	I2S data
B2	I2S_WS	I/O	I2S L/R word select
E3	SPI_CLK	I	SPI clcock
E4	SPI_DATA	I	SPI data
D3	SPI_ENABLE	I	SPI Enable
E2	MCLK/XTAL_IN	I	Master Clock / Xtal input
D2	XTAL_OUT	O	Xtal output
C4	BYPASS	I/O	Analog VDD/2 bypass capacitor connection point
B4	AV_{DD}	P	Analog supply
A3	AGND	P	Analog Ground
C1	DV_{DD}	P	Digital Supply
A1	GNDD	P	Digital ground
D1	VDDX	P	XTAL Oscillator circuit supply
E1	GNDX	P	XTAL Oscillator circuit ground
B3	HP_L	O	HP left output
A4	HP_R	O	HP right output
A2	No Connect	O	Must let float
C3	No Connect	NC	NC
D4	No Connect	NC	NC

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		-0.3V to V_{DD} + 0.3V
Power Dissipation[3]		Internally Limited
ESD Susceptibility	Human body model[4]	2000V
	Machine model[5]	200V
Junction Temperature		150°C
Thermal Resistance	θ_{JA}	60°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the GND pin, unless otherwise specified.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine Model, 220pF – 240pF discharged through all pins.

Operating Ratings

Temperature Range		
$T_{MIN} \le T_A \le T_{MAX}$		−40°C ≤ T_A ≤ 85°C
Supply Voltage	DV_{DD}	2.6V ≤ DV_{DD} ≤ 5.0V
	AV_{DD}	2.6V ≤ AV_{DD} ≤ 5.5V

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Electrical Characteristics DV_{DD} = 3.0V, AV_{DD} = 5.0V, R_L = 32Ω(1)(2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4921		Units (Limits)
			Typical(3)	Limit(4)(5)	
DV_{DD}	Digital Power Supply Voltage	See (6)	3.0		V
AV_{DD}	Analog Power Supply Voltage	See (6)	5.0		V
DI_{DD}	Digital Power Supply Quiescent Current	R_{Load} = ∞, f_{MLCK} = 11.2896MHz	3.5	7.5	mA (max)
AI_{DD}	Analog Power Supply Quiescent Current	R_{Load} = ∞, f_{MCLK} = 0MHz	6	10	mA (max)
I_{SD}	Total Shutdown Power Supply Current	SHUTDOWN SPI bits 1 & 2 set to logic 0, SPI, M_{CLK} and I^2S inputs at GND	1	5	uA(max)
I_{SB}	Standby Current	Analog and Digital together All clocks off	25		uA
V_{FS}	Full-Scale Output Voltage	Gain set at max	3.5		V_{P-P}
THD+N	Total Harmonic Distortion + Noise	f_{IN} = 1kHz, P_{OUT} = 12mW (Vol Control = 11111, I^2S input adj to get 12mW at output)	0.03		%
P_O	Headphone Amplifier Output Power	THD = (0.5%), f_{OUT} = 1kHz	50	40	mW (min)
PSRR	Power Supply Rejection Ratio	AV_{DD} C_{BYPASS} = 2.0µF V_{RIPPLE} = 200mV_{P-P} 217Hz	62	45	dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 1kHz sinewave at -60dB_{FS}, A-weighted-f_{CONV} = 44.1kHz	82		dB
DR	Dynamic Range	f_{IN} = 1kHz sinewave at -60dB_{FS}, A-weighted	84		dB
ΔA_{CH-CH}	Channel-to-Channel Gain Mismatch	f_{IN} = 1kHz	0.06		dB
X_{TALK}	Channel-to-Channel Crosstalk	f_{CONV} = 44.1kHz, f_{IN} = 1kHz sinewave at -3dB_{FS}	72		dB
	Volume Control Range	Minimum Attenuation Maximum Attenuation	+3.0 -43.5		dB dB
	Volume Control Control Step Size		1.5		dB
	Mute Attenuation		-102		dB

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(2) All voltages are measured with respect to the GND pin, unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) Best operation is achieved by maintaining 3.0V ≤ AV_{DD} ≤ 5.0V and 3.0V ≤ DV_{DD} ≤ 5.0V.

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Electrical Characteristics DV_{DD} = 3.0V, AV_{DD} = 3.0V, R_L = 32Ω(1)(2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4921		Units (Limits)
			Typical(3)	Limit(4)(5)	
DV_{DD}	Digital Power Supply Voltage	See (6)	3.0		V
AV_{DD}	Analog Power Supply Voltage	See (6)	3.0		V
DI_{DD}	Digital Power Supply Quiescent Current	R_{Load} = ∞, f_{MLCK} = 11.2896MHz	3.5	7.5	mA (max)
AI_{DD}	Analog Power Supply Quiescent Current	R_{Load} = ∞, f_{MCLK} = 0MHz	5	9.0	mA (max)
I_{SD}	Total Shutdown Power Supply Current	SHUTDOWN SPI bits 1 & 2 set to logic 0, SPI, M_{CLK} and I^2S inputs at GND	1		uA(max)
I_{SB}	Standby Current	Analog and Digital together All clocks off	15		uA
V_{FS}	Full-Scale Output Voltage	Gain set at max	2.6		V_{P-P}
THD+N	Total Harmonic Distortion + Noise	f_{IN} = 1kHz, P_{OUT} = 12mW (Vol Cont = 11011, I^2S input adj to get 12mW at output)	0.05		%
P_O	Headphone Amplifier Output Power	THD = (0.5%), f_{OUT} = 1kHz	26		mW (min)
PSRR	Power Supply Rejection Ratio	AV_{DD} C_{BYPASS} = 2.0µF V_{RIPPLE} = 200mV_{P-P} 217Hz	52		dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 1kHz sinewave at -60dB_{FS}, A-weighted-f_{CONV} = 44.1kHz	79		dB
DR	Dynamic Range	f_{IN} = 1kHz sinewave at -60dB_{FS}, A-weighted	81		dB
ΔA_{CH-CH}	Channel-to-Channel Gain Mismatch	f_{IN} = 1kHz	0.06		dB
X_{TALK}	Channel-to-Channel Crosstalk	f_{CONV} = 44.1kHz, f_{IN} = 1kHz sinewave at -3dB_{FS}	72		dB
	Volume Control Range	Minimum Attenuation Maximum Attenuation	0 -43.5		dB dB
	Volume Control Control Step Size		1.5		dB
	Mute Attenuation		-100		dB

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the GND pin, unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) Best operation is achieved by maintaining 3.0V ≤ AV_{DD} ≤ 5.0V and 3.0V ≤ DV_{DD} ≤ 5.0V.

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Electrical Characteristics-Digital Inputs DV_{DD} = 3.0V(1)(2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4921		Units (Limits)
			Typical(3)	Limit(4)(5)	
	Resolution		16		Bits
I^2S	Audio Data Interface Format	Standard, I^2S, Left Justified			
f_{MCLK}	Master Clock Frequency		11.2896 (256FS)		MHz
f_{CONV}	Sampling Clock Frequency Range		44.1	48	kHz
V_{IL}	Digital Input: Logic Low Voltage Level			0.3 X DV_{DD}	V (max)
V_{IH}	Digital Input: Logic High Voltage Level			0.7 X DV_{DD}	V (min)
t_{ES}	SPI_ENB Setup Time			20	ns (min)
t_{EH}	SPI_ENB Hold Time			20	ns (min)
t_{EL}	SPI_ENB Low Time			30	ns (min)
t_{DS}	SPI_Data Setup Time			20	ns (min)
t_{DH}	SPI_Data Hold Time			20	ns (min)
t_{CS}	SPI_CLK Setup Time			20	ns (min)
t_{CH}	SPI_CLK High Pulse Width			100	ns (min)
t_{CL}	SPI_CLK Low Pulse Width			100	ns (min)
f_{CLK}	SPI_CLK Frequency			5	MHz (max)
t_{CLKI^2S}	I^2S_CLK Period			50	ns (min)
t_{HII^2S}	I^2S_CLK High Pulse Width			20	ns (min)
t_{LOI^2S}	I^2S_CLK Low Pulse Width			20	ns (min)
	I^2S_LRCLK Duty Cycle		50		%
t_{SLRCLK}	I^2S_LRCLK to I^2S_CLK Setup Time			20	ns (min)
t_{HLRCLK}	I^2S_LRCLK to I^2S_CLK Hold Time			20	ns (min)
t_{SDI^2S}	I^2S_Data to I^2S_CLK Setup Time			20	ns (min)
t_{HDI^2S}	I^2S_Data to I^2S_CLK Hold Time			20	ns (min)

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(2) All voltages are measured with respect to the GND pin, unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

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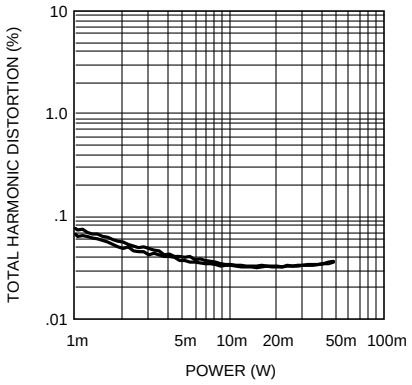
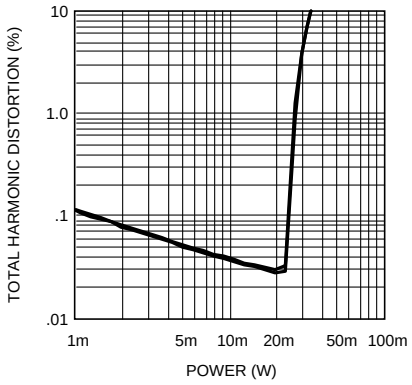
Typical Performance Characteristics

THD+N vs Output Power



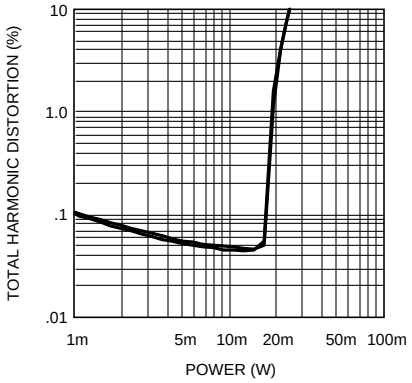
1. Analog V_{DD} = 5V, Digital V_{DD} = 3V
R_L = 32Ω, 44.1 kHz Sample Rate
R & L Channels, Vol = 3dB, Frequency in = 1kHz
Figure 3.

THD+N vs Output Power



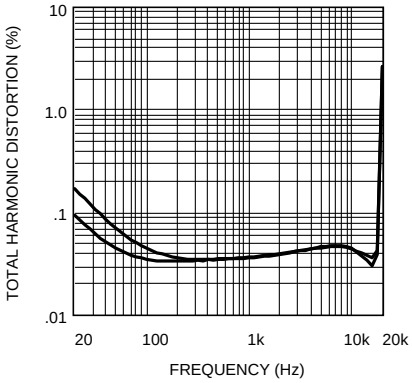
Analog V_{DD} = 3V, Digital V_{DD} = 3V
R_L = 32Ω, 44.1 kHz Sample Rate R & L Channels Shown
Vol = 3dB, Frequency in = 1kHz
Figure 4.

THD+N vs Output Power



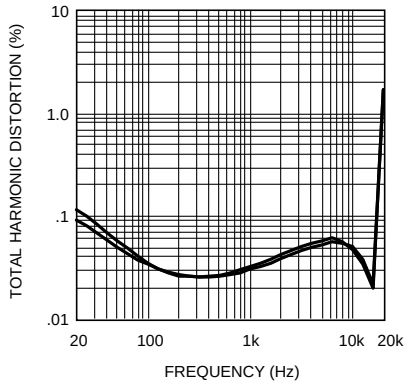
Analog V_{DD} = 2.6V, Digital V_{DD} = 2.6V
R_L = 32Ω, 4.1 kHz Sample Rate
R & L Channels Shown, Vol = 3dB, Frequency in = 1kHz
Figure 5.

THD+N vs Frequency



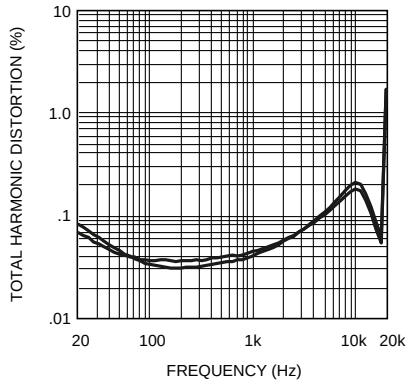
Analog V_{DD} = 5V, Digital V_{DD} = 3V
R_L = 32Ω, Power Level = 50mW,
R & L Channels Shown , 44.1kHz Sample Rate
Figure 6.

THD+N vs Frequency



Analog V_{DD} = 3V, Digital V_{DD} = 3V
R_L = 32Ω, Power Level = 12mW
R & L Channels Shown, 44.1kHz Sample Rate
Figure 7.

THD+N vs Frequency



Analog V_{DD} = 2.6V, Digital V_{DD} = 2.6V
R_L = 32Ω, Power Level = 12mW
R & L Channels Shown, 44.1kHz Sample Rate
Figure 8.

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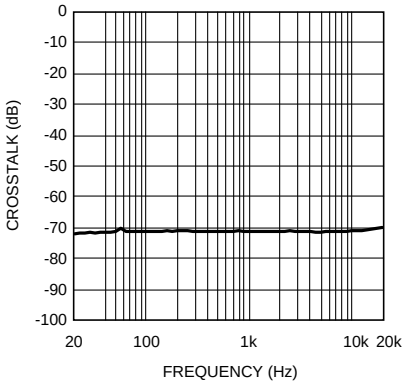
Typical Performance Characteristics (continued)

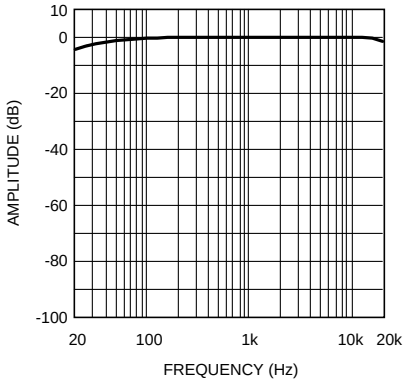
Crosstalk



Analog V_{DD} = 3V, Digital V_{DD} = 3V
RL = 32Ω, Vol = 3dB
44.1kHz Sample Rate, -3dB FFS

Figure 9.

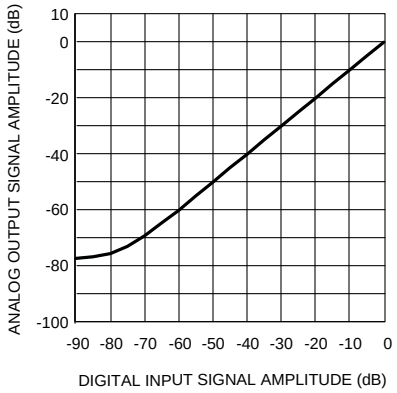
Frequency Response



Analog V_{DD} = 5V, Digital V_{DD} = 3V
RL = 32Ω, Vol = 0dB
44.1kHz Sample Rate, 0dB FFS

Figure 10.

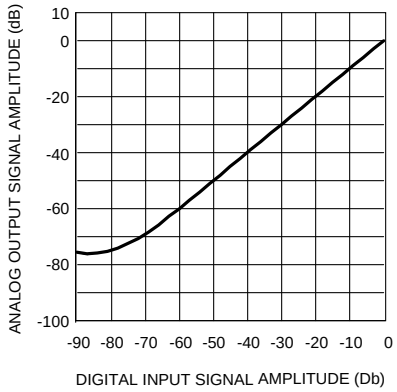
Linearity



Analog V_{DD} = 5V, Digital V_{DD} = 3V
R_L = 32Ω, 44.1kHz Sample Rate

Figure 11.

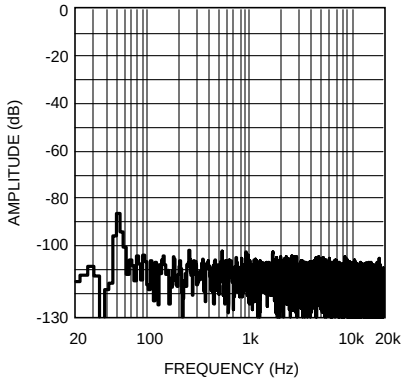
Linearity



Analog V_{DD} = 3V, Digital V_{DD} = 3V
R_L = 32Ω, 44.1kHz Sample Rate

Figure 12.

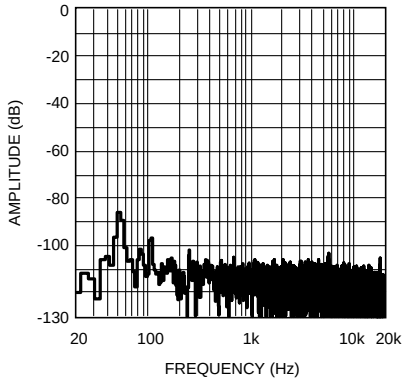
Noise Floor



Analog V_{DD} = 5V, Digital V_{DD} = 3V
R_L = 32Ω, Vol = 3dB
44.1kHz Sample Rate

Figure 13.

Noise Floor



Analog V_{DD} = 3V, Digital V_{DD} = 3V
R_L = 32Ω, Vol = 0dB
44.1kHz Sample Rate

Figure 14.

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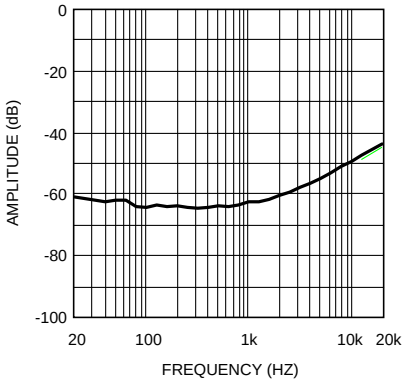
Typical Performance Characteristics (continued)

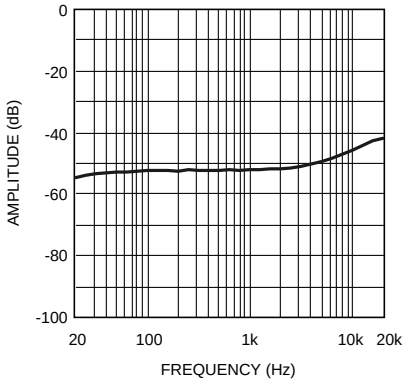
PSRR vs Frequency



Analog V_{DD} = 5V, Digital V_{DD} = 3V
R_L = 32Ω, Vol = 3dB
44.1kHz Sample Rate

Figure 15.

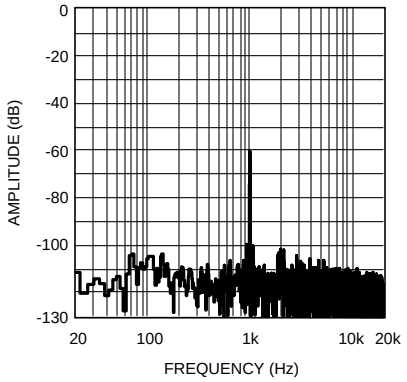
PSRR vs Frequency



Analog V_{DD} = 3V, Digital V_{DD} = 3V
R_L = 32Ω, Vol = 0dB
44.1kHz Sample Rate

Figure 16.

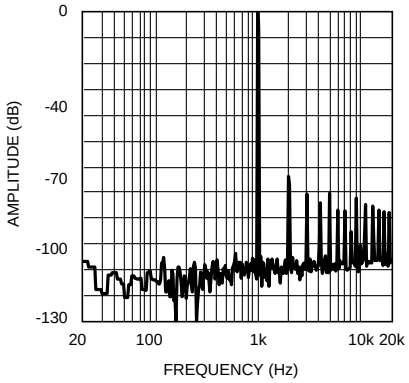
FFT @ 1kHz -60dB



Analog V_{DD} = 5V, Digital V_{DD} = 3V
R_L = 32Ω, Vol = 3dB
44.1kHz Sample Rate

Figure 17.

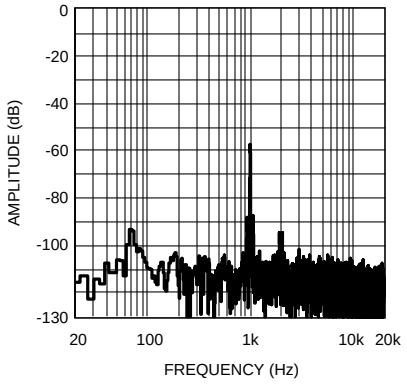
FFT @ 1kHz 0dB



Analog V_{DD} = 5V, Digital V_{DD} = 3V
RL = 32Ω, Vol = 3dB
44.1 kHz Sample Rate

Figure 18.

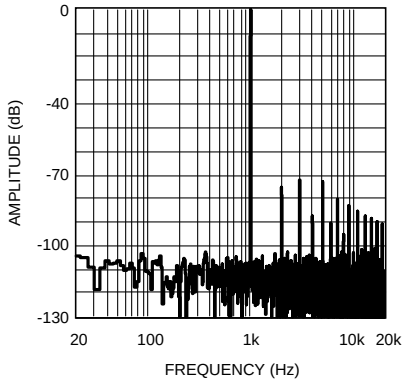
FFT @ 1kHz -60dB



Analog V_{DD} = 3V, Digital V_{DD} = 3V
R_L = 32Ω, Vol = 0dB
44.1kHz Sample Rate

Figure 19.

FFT @ 1kHz 0dB



Analog V_{DD} = 3V, Digital V_{DD} = 3V
R_L = 32Ω, Vol = 0dB
44.1kHz Sample Rate

Figure 20.

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APPLICATION INFORMATION

SPI OPERATIONAL DESCRIPTION

The serial data bits are organized into a field which contains 16 bits of data defined by Table 1. Bits 1 & 2 determine the output mode of the LM4921 as shown in Table 2. Bits 7 through 11 determine the volume level setting as illustrated by Table 3. Bit 12 sets the Bypass capacitor charging time.

Table 1. Bit Allocation

BIT #	Default Val	Function	Description
0 (LSB)	0	RESET_B	RESET_B = 0, Resets the DAC Must be high for the part to run.
1	0	MODE CONTROL	See Table 2
2	0		
3	0	MASTER/SLAVE	0 = SLAVE, 1 = MASTER
4	0	RESOLUTION	0 = 16 bit, 1 = 32 bit
5	0	RESERVED	Should always be set to '1'
6	0	ZERO CROSSING SET	0 = ZXD ENABLE, 1 = ZXD DISABLE
7	0	VOLUME CONTROL	See Table 3
8	0		
9	0		
10	0		
11	0		
12	0	BYP CHARGE RATE	0 = 1X, 1 = 2X
13	0	RESERVED	
14	0	RESERVED	
15 (MSB)	0	RESERVED	Should always be set to '0'

MODE CONTROL

Sets the modes as outlined in Table 2.

Table 2. Output Mode Selection (Bits 1 & 2 above)

Output Mode #	BIT 2	BIT 1	MODE
0	0	0	SD
1	0	1	STANDBY
2	1	0	MUTE
3	1	1	ACTIVE

Shutdown turns off the part completely for maximum power savings. The Standby mode turns off the clock but still consumes more power than the shutdown mode. However, coming out of standby mode allows the part to turn back on faster than from shutdown. In Mute mode the clocks remain on which uses more power but allows faster recovery and the ability to supply clock signals to other devices which is important when the part is used in master mode. Active mode turns the part on for normal operation.

MASTER/SLAVE SELECT

Allows the part to act as a master and supply the clock for the rest of the system or be a slave to the system clock.

RESOLUTION SET

Sets the resolution to be either 16 or 32 bits of stereo audio information. For most applications this will be set at 16 bits.

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ZERO CROSSING DETECT SET

This pin turns on the zero crossing detection circuit. With this circuit enabled the part will not allow a volume step change, or shutdown mode, or standby mode to occur until the audio input signal passes through zero. This pin should be set to on for most applications.

VOLUME CONTROL

The internal Stereo Volume Control is set by changing bits 7 through 11 in the SPI interface, as shown in Table 3 below. The zero dB setting is for 3V VDD operation and the +3dB is for 5V VDD.

Table 3. Volume Control Settings

Gain (dB) HP_L & HP_R	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7
-43.5	0	0	0	0	0
-42.0	0	0	0	0	1
-40.5	0	0	0	1	0
-39.0	0	0	0	1	1
-37.5	0	0	1	0	0
-36.0	0	0	1	0	1
-34.5	0	0	1	1	0
-33.0	0	0	1	1	1
-31.5	0	1	0	0	0
-30.0	0	1	0	0	1
-28.5	0	1	0	1	0
-27.0	0	1	0	1	1
-25.5	0	1	1	0	0
-24.0	0	1	1	0	1
-22.5	0	1	1	1	0
-21.0	0	1	1	1	1
-19.5	1	0	0	0	0
-18.0	1	0	0	0	1
-16.5	1	0	0	1	0
-15.0	1	0	0	1	1
-13.5	1	0	1	0	0
-12.0	1	0	1	0	1
-10.5	1	0	1	1	0
-9.0	1	0	1	1	1
-7.5	1	1	0	0	0
-6.0	1	1	0	0	1
-4.5	1	1	0	1	0
-3.0	1	1	0	1	1
-1.5	1	1	1	0	0
0.0	1	1	1	0	1
1.5	1	1	1	1	0
3.0	1	1	1	1	1

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BYPASS CHARGE RATE BIT 12

This control pin allows the user to change the Bypass Capacitor's charge rate by a factor of two. Setting this bit at zero will set the circuit to it's normal 1x rate. Setting the bit to High will double the charge rate and allow the part to turn on faster with a slight degradation in turn on click/pop noise.

BITS 5, 13, 14, and 15

Bits 13, 14, and 15 are all reserve bits and must be set to low/zero/ground.

Bit 5 must be set High.

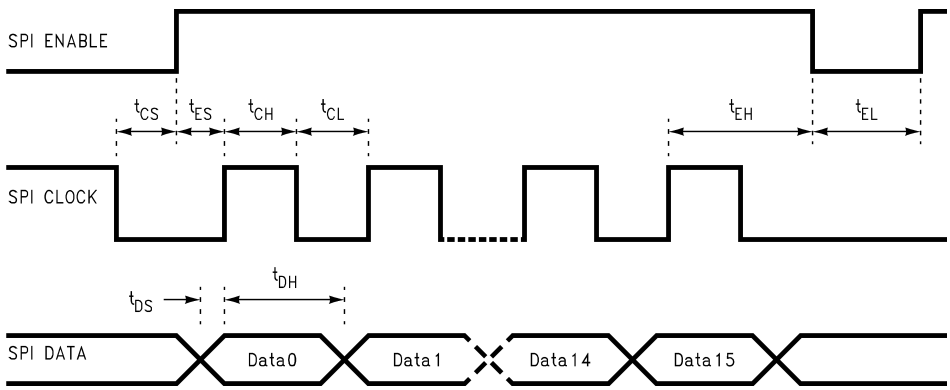
SPI CONTROL INTERFACE BUS (J1)

SPI DATA: This is the serial data pin.

SPI CLK: This is the clock input pin.

SPI ENABLE: This is the SPI enable pin.

SPI TIMING DIAGRAM



SPI OPERATIONAL REQUIREMENTS

1. The maximum clock rate is 5MHz for the CLK pin.

2. CLK must remain logic-high for at least 100ns (t_{CH}) after the rising edge of CLK, and CLK must remain logic-low for at least 100ns (t_{CL}) after the falling edge of CLK.

3. Data bits are written to the DATA pin with the least significant bit (LSB) first.

4. The serial data bits are sampled at the rising edge of CLK. Any transition on DATA must occur at least 20ns (t_{DS}) before the rising edge of CLK. Also, any transition on DATA must occur at least 20ns (t_{DH}) after the rising edge of CLK and stabilize before the next rising edge of CLK.

5. ENABLE should be logic-high only during serial data transmission.

6. ENABLE must be logic-high at least 20ns (t_{ES}) before the first rising edge of CLK, and ENABLE has to remain logic-high at least 20ns (t_{EH}) after the sixteenth rising edge of CLK.

7. If ENABLE remains logic-low for more than 10ns before all 16 bits are transmitted then the data latch will be aborted.

8. If ENABLE is logic-high for more than 16 CLK pulses then only the first 16 data bits will be latched and activated at rising edge of sixteenth CLK.

9. ENABLE must remain logic-low for at least 30ns (t_{EL}).

10. Coincidental rising or falling edges of CLK and ENABLE are not allowed. If CLK is to be held logic-high after the data transmission, the falling edge of CLK must occur at least 20ns (t_{CS}) before ENABLE transitions to logic-high for the next set of data.

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I2S INTERFACE BUS (J2 - See Figure 21)

The I2S standard provides a uni-directional serial interface designed specifically for digital audio. For the LM4921, the interface provides access to a 48kHz, 16 bit full-range stereo audio DAC. This interface uses a three wire system of clock (I2S_CLK), data (I2S_DATA), and word select (I2S_WS, sometimes called Right/Left Select).

A bit clock (I2S_CLK) at 32 or 64 times the sample frequency is established by the I2S system master and the word select (I2S_WS) line is driven at a frequency equal to the sampling rate of the audio data, in this case 48kHz. The word line is registered to change on the positive edge of the bit clock. The serial data (I2S_DATA) is sent MSB first, again registers on the positive edge of the bit clock, delayed by 1 bit clock cycle relative to the changing of the word line (typical I^2S format).

MCLK/XTAL_IN (S1 MCLK SEL - See Figure 21)

This is the input for an external Master Clock. The jumper at S1 must be removed (disconnecting the onboard crystal from the circuit) when using an external Master Clock.

STEREO HEADPHONE OUTPUT JACK (J3 - See Figure 21)

This is the stereo headphone output. Each channel is single-ended, with 100uF DC output blocking capacitors mounted on the demo board (C6 and C7). These capacitors are necessary to block the 1/2 VDD DC bias and prevent it from flowing through the headphone speakers (DC current will destroy most audio speakers) while allowing the audio ac signal to pass through. The jack features a typical stereo headphone pinout.

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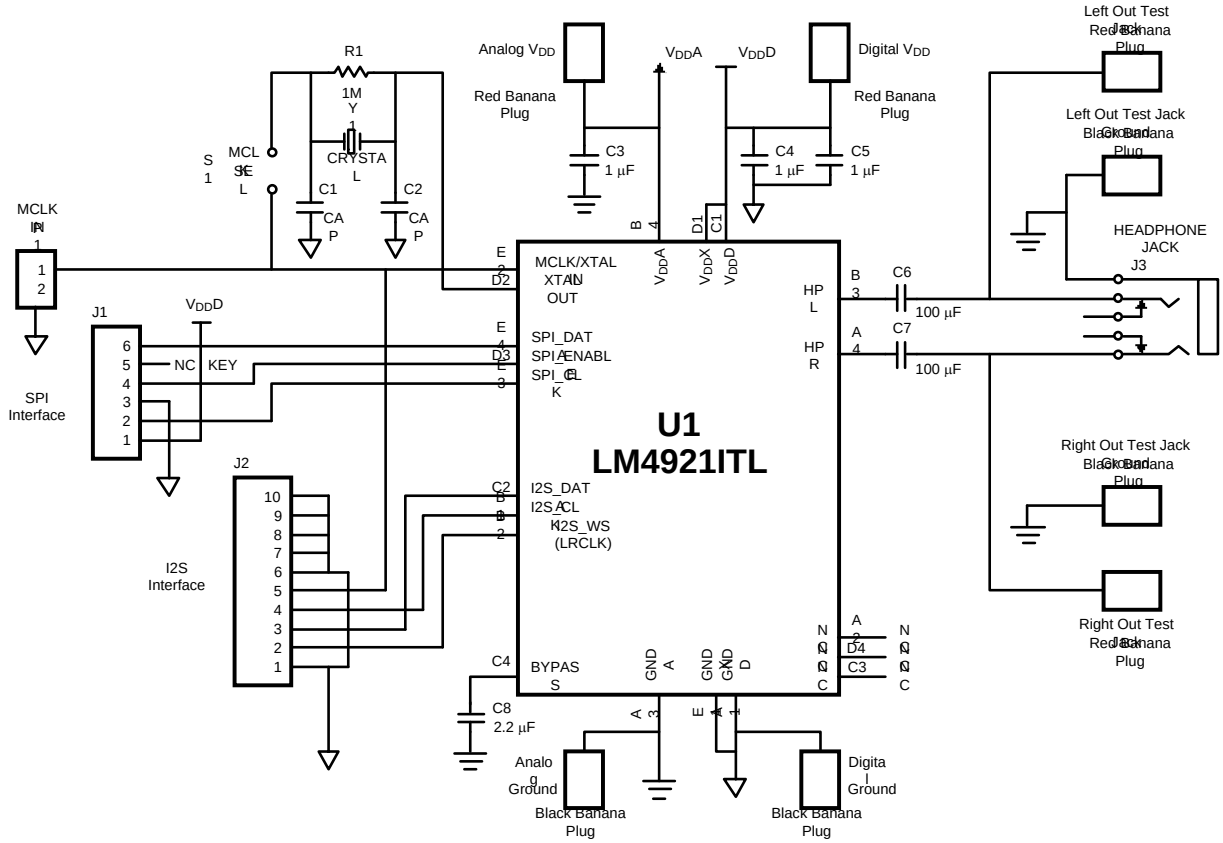
LM4921ITL DEMO BOARD OPERATION

The LM4921ITL demo board is a complete evaluation platform (Parallel Port SPI Interface Card and control software available), designed to give easy access to the control pins of the part and comprise all the necessary external passive components. There are separate analog and digital supply connectors, SPI interface bus (J1) for the control lines, I^2S interface bus (J2) for full-range digital audio, stereo headphone output (J3), and an external MCLK input (P1) for use in place of the crystal on the demoboard.



(1) Parallel Port SPI Interface Card and control software available.

Figure 21. LM4921ITL Demo Board Schematic

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DEMO BOARD BILL OF MATERIALS

Texas Instruments Bill of Material				
Analog Audio LM4921ITL20 Eval Board				
Assembly Part Number: 980011973-100				
Revision A				
Item	**Part Number**	**Part Description**	**Qty**	**Ref Designator**
1	551011973-001	LM4921 Eval Board PCB etch 001	1	
2		LM4921 ITL20 DSBGA 20 Bumps	1	U1
3		Cer Cap 22pF 50V 10%, size 1206	2	C1, C2
4		Cer Cap 0.1pF 50V 10%, size 1206	1	C4
5		Tant Cap 1µF 16V 10%, 3216	3	C3, C5, C8
6		Tant Cap 220µF 16V 10%, 7243	2	C6, C7
7		1 meg ohm	1	R1
8		Crystal 11.2896MHz	1	Y1
9		Phone Jack 3.5mm Stereo	1	J3
10		Jumper Header 1X2	2	P1, S1
11		Jumper Header 1X3	2	J1
12		Jumper Header 1X5	2	J2
13		PCB Banana Jack, Black-Mouser 164-6218	4	A GND, D GND, GND (2)
14		PCB Banana Jack, Red-Mouser 164-6219	4	A VDD, D VDD, HP L, HP R

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DEMO BOARD ARTWORKS

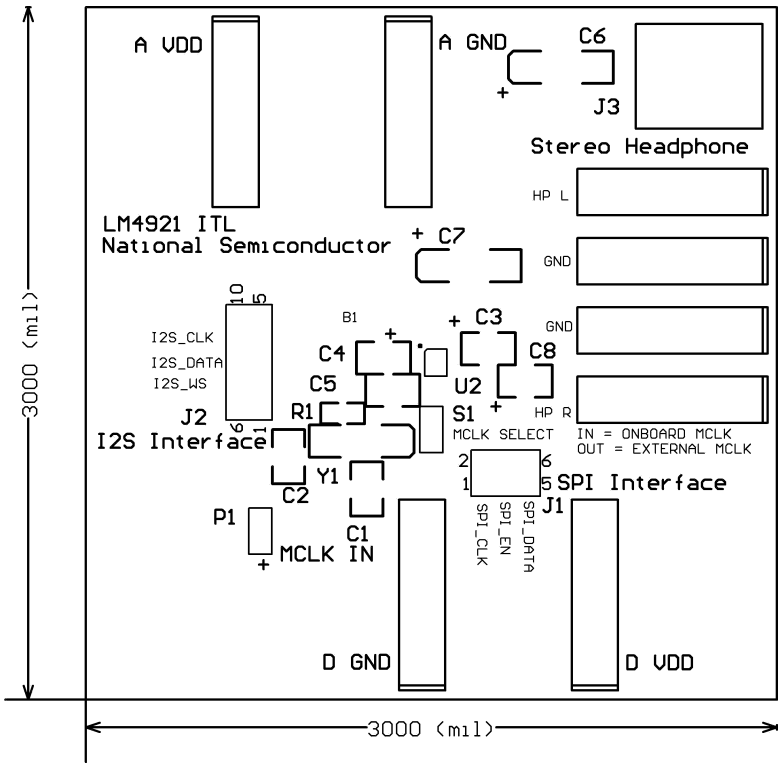

Figure 22. Silkscreen Layer

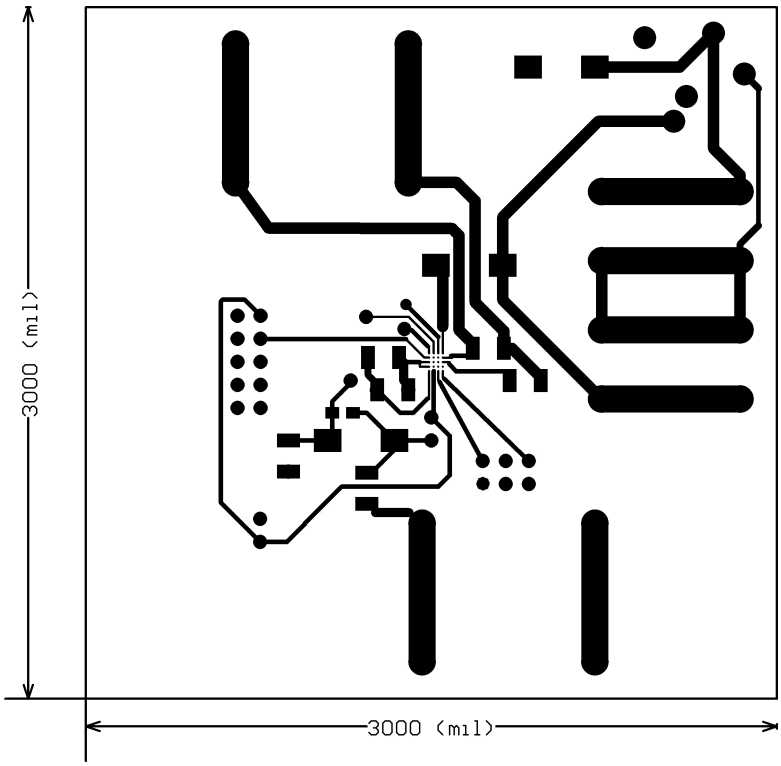

Figure 23. Top Layer

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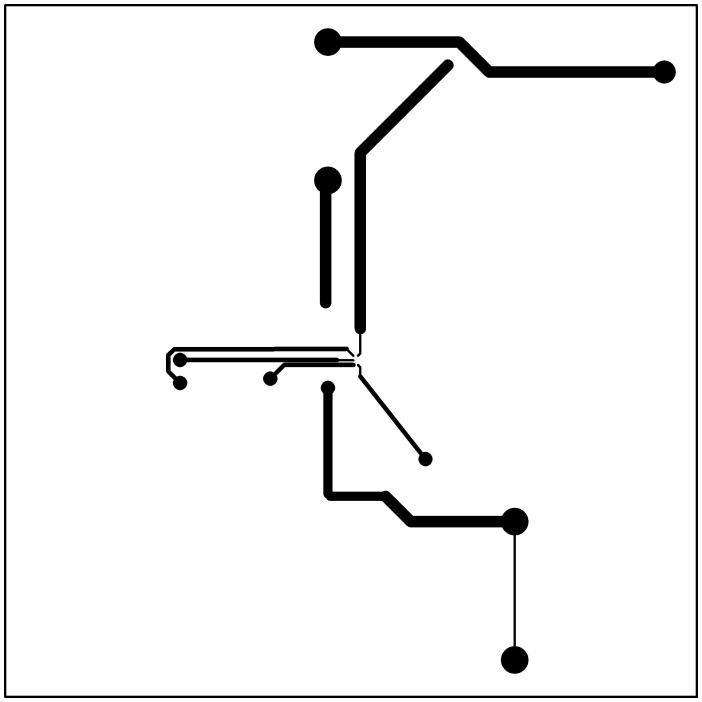

Figure 24. Mid Layer 1

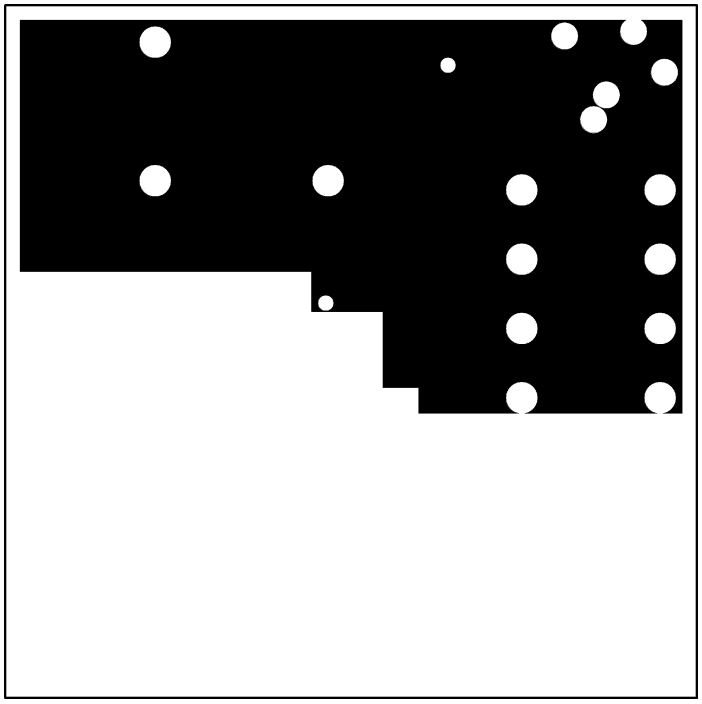

Figure 25. Mid Layer 2

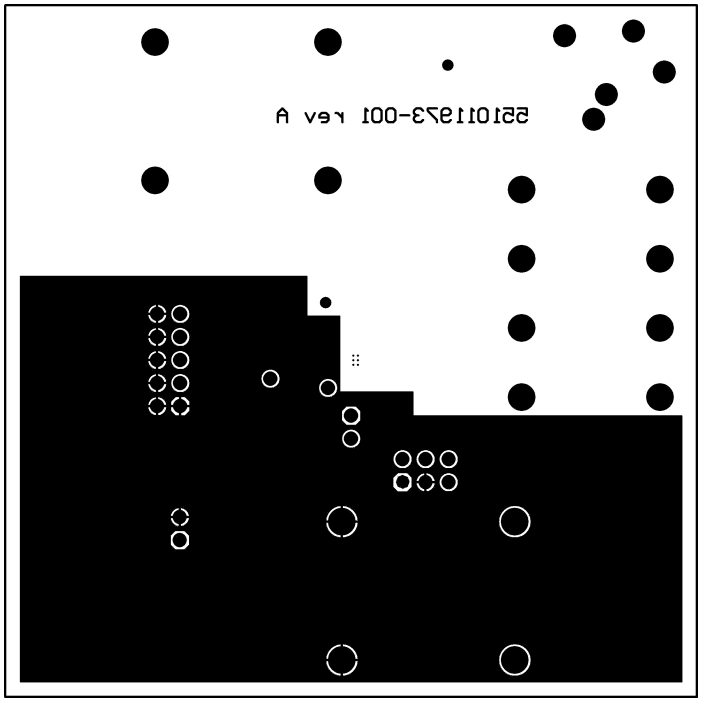

Figure 26. Bottom Layer

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REVISION HISTORY

Changes from Revision D (May 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4921ITL/NOPB	ACTIVE	DSBGA	YZR	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	G B9	Samples
LM4921ITLX/NOPB	ACTIVE	DSBGA	YZR	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	G B9	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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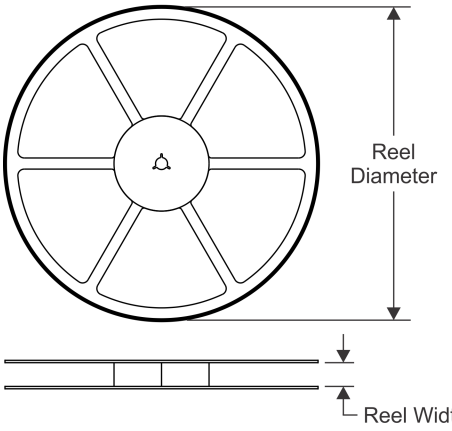
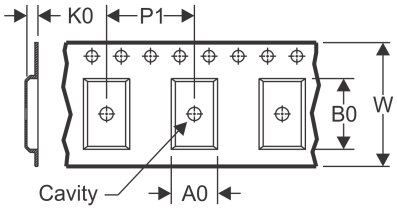
TAPE AND REEL INFORMATION

REEL DIMENSIONS

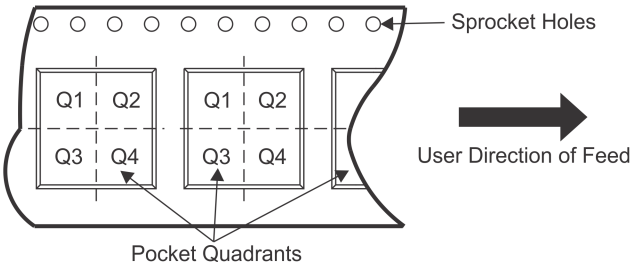


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

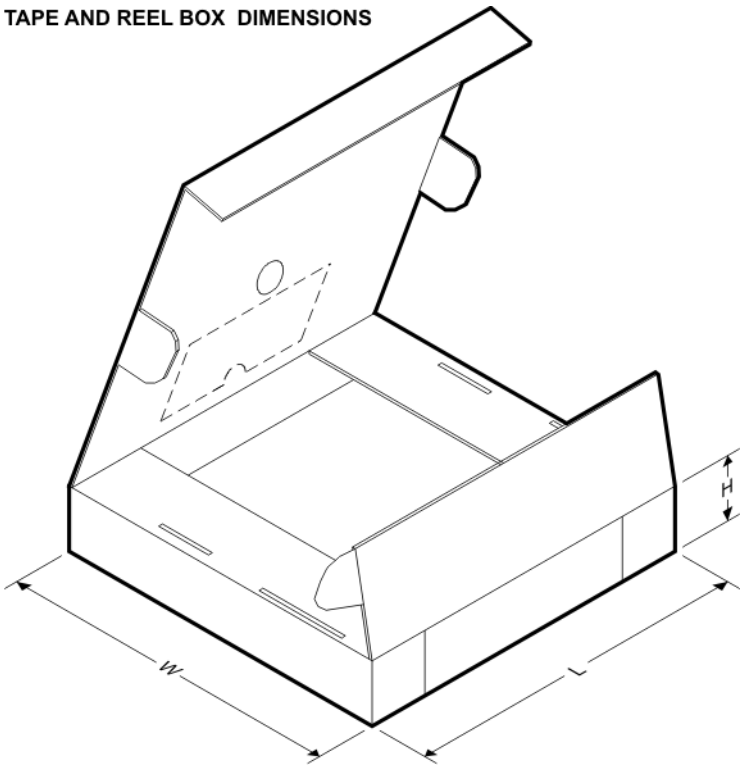
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4921ITL/NOPB	DSBGA	YZR	20	250	178.0	8.4	2.34	2.85	0.76	4.0	8.0	Q1
LM4921ITLX/NOPB	DSBGA	YZR	20	3000	178.0	8.4	2.34	2.85	0.76	4.0	8.0	Q1

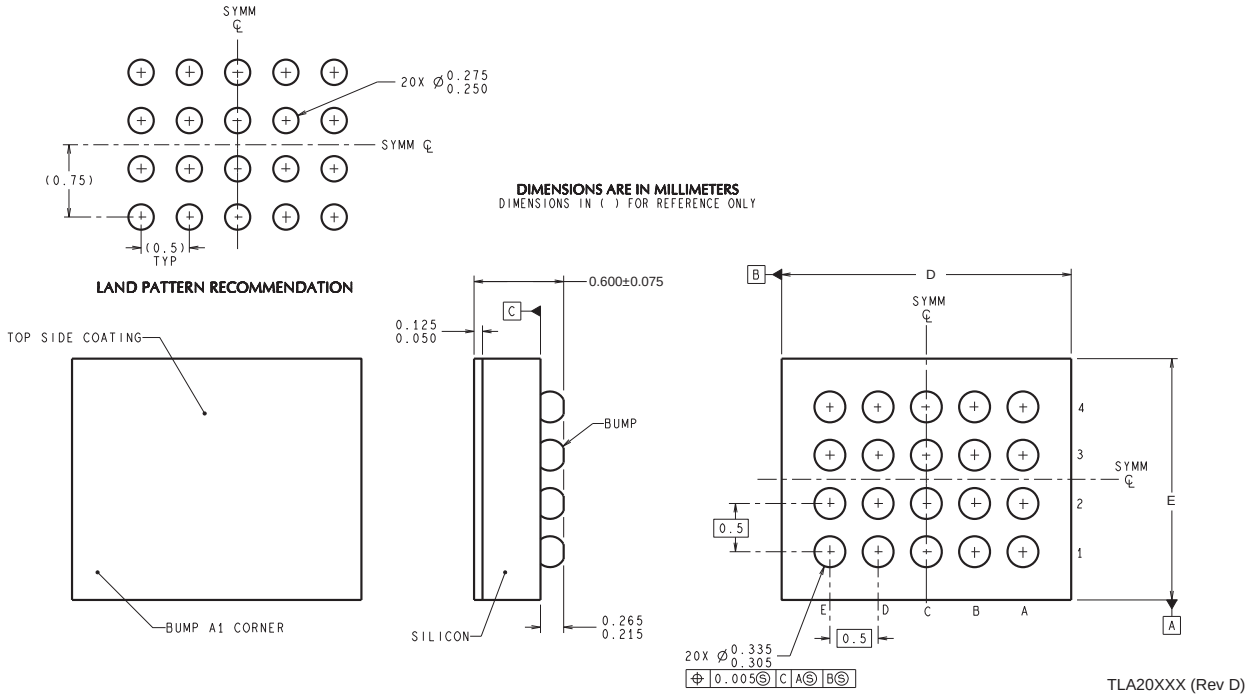
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4921ITL/NOPB	DSBGA	YZR	20	250	210.0	185.0	35.0
LM4921ITLX/NOPB	DSBGA	YZR	20	3000	210.0	185.0	35.0

YZR0020



D: Max = 2.772 mm, Min =2.711 mm

E: Max = 2.238 mm, Min =2.177 mm

4215053/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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