LM4766 *Overture*™ Audio Power Amplifier Series Dual 40W Audio Power Amplifier with Mute

Check for Samples: LM4766

FEATURES

- **SPiKe Protection**
- **Minimal Amount of External Components Necessary**
- **Quiet Fade-In/Out Mute Mode**
- **Non-Isolated 15-Lead TO-220 Package**
- **Wide Supply Range 20V - 78V**

APPLICATIONS

- **High-End Stereo TVs**
- **Component Stereo**
- **Compact Stereo**

KEY SPECIFICATIONS

- **THD+N at 1kHz at 2 x 30W Continuous Average Output Power Into 8Ω 0.1% (Max)**
- **THD+N at 1kHz at Continuous Average Output Power of 2 x 30W Into 8Ω 0.009% (Typ)**

DESCRIPTION

The LM4766 is a stereo audio amplifier capable of delivering typically 40W per channel with the non-isolated "NDL" package and 30W per channel with the isolated "NDB" package of continuous average output power into an 8Ω load with less than 0.1% (THD+N).

The performance of the LM4766, utilizing its Self Peak Instantaneous Temperature (°Ke) (SPiKe) Protection Circuitry, places it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** Protection means that these parts are safeguarded at the output against overvoltage, undervoltage, overloads, including thermal runaway and instantaneous temperature peaks.

Each amplifier within the LM4766 has an independent smooth transition fade-in/out mute that minimizes output pops. The IC's extremely low noise floor at 2µV and its extremely low THD+N value of 0.06% at the rated power make the LM4766 optimum for high-end stereo TVs or minicomponent systems.

Connection Diagram

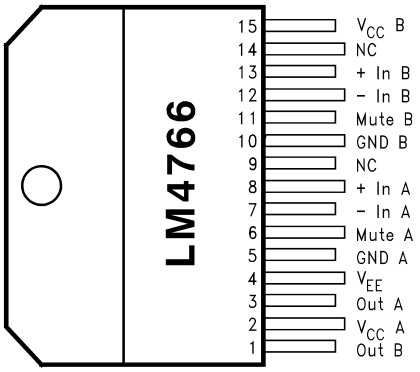

Figure 1. Plastic Package
Top View
Non-Isolated TO-220 Package
See Package Number NDL0015A
Isolated PFM Package
See Package Number NDB0015B

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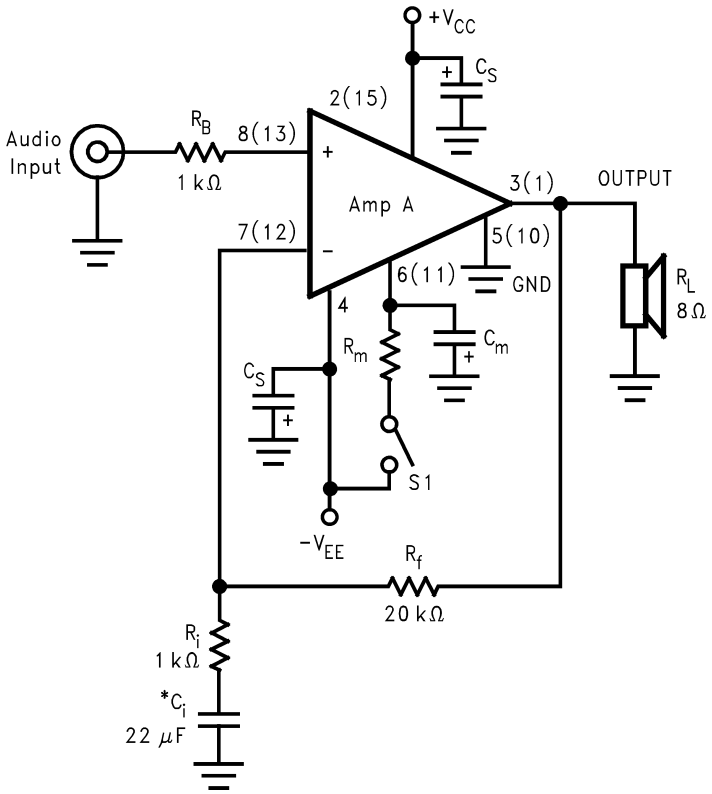
Typical Application



Numbers in parentheses represent pinout for amplifier B.
*Optional component dependent upon specific design requirements.

Figure 2. Typical Audio Amplifier Application Circuit

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1) (2) (3)

Supply Voltage $\|V_{CC}\| + \|V_{EE}\|$		(No Input)	78V
		(with Input)	74V
Common Mode Input Voltage			(V_{CC} or V_{EE}) and $\|V_{CC}\| + \|V_{EE}\| \le 60V$
Differential Input Voltage			60V
Output Current			Internally Limited
Power Dissipation (4)			62.5W
ESD Susceptibility (5)			3000V
Junction Temperature (6)			150°C
Thermal Resistance	Non-Isolated NDL-Package	θ_{JC}	1°C/W
	Isolated NDB-Package	θ_{JC}	2°C/W
Soldering Information		NDL and NDB Packages	260°C
Storage Temperature			−40°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) All voltages are measured with respect to the GND pins (5, 10), unless otherwise specified.
(4) For operating at case temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of θ_{JC} = 1°C/W (junction to case) for the NDL package. Refer to the section DETERMINING THE CORRECT HEAT SINK in the APPLICATION INFORMATION section.
(5) Human body model, 100pF discharged through a 1.5kΩ resistor.
(6) The operating junction temperature maximum is 150°C, however, the instantaneous Safe Operating Area temperature is 250°C.

OPERATING RATINGS (1) (2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-20°C \le T_A \le +85°C$
Supply Voltage $\|V_{CC}\| + \|V_{EE}\|$ (3)		20V to 60V

(1) All voltages are measured with respect to the GND pins (5, 10), unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Operation is ensured up to 60V, however, distortion may be introduced from **SPiKe** Protection Circuitry if proper thermal considerations are not taken into account. Refer to the APPLICATION INFORMATION section for a complete explanation.

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ELECTRICAL CHARACTERISTICS (1) (2)

The following specifications apply for V_{CC} = +30V, V_{EE} = −30V, I_{MUTE} = −0.5mA with R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4766		Units (Limits)
			Typical (3)	Limit (4)	
$\|V_{CC}\| + \|V_{EE}\|$	Power Supply Voltage (5)	GND − V_{EE} ≥ 9V	18	20	V (min)
				60	V (max)
P_O (6) (7)	Output Power (Continuous Average)	NDL Package, V_{CC} = ±30V,THD+N = 0.1% (max), f = 1kHz, f = 20kHz	40	30	W/ch (min)
		NDB Package, V_{CC} = ±26V(7), THD+N = 0.1% (max), f = 1kHz, f = 20kHz	30	25	W/ch (min)
THD+N	Total Harmonic Distortion Plus Noise	NDL Package, 30W/ch, R_L = 8Ω, 20Hz ≤ f ≤ 20kHz, A_V = 26dB	0.06		%
		NDB Package, 25W/ch, R_L = 8Ω, 20Hz ≤ f ≤ 20kHz, A_V = 26dB	0.06		%
X_{talk}	Channel Separation	f = 1kHz, V_O = 10.9Vrms	60		dB
SR (6)	Slew Rate	V_{IN} = 1.2Vrms, t_{rise} = 2ns	9	5	V/μs (min)
I_{total} (8)	Total Quiescent Power Supply Current	Both Amplifiers V_{CM} = 0V, V_O = 0V, I_O = 0mA	48	100	mA (max)
V_{OS} (8)	Input Offset Voltage	V_{CM} = 0V, I_O = 0mA	1	10	mV (max)
I_B	Input Bias Current	V_{CM} = 0V, I_O = 0mA	0.2	1	μA (max)
I_{OS}	Input Offset Current	V_{CM} = 0V, I_O = 0mA	0.01	0.2	μA (max)
I_O	Output Current Limit	$\|V_{CC}\| = \|V_{EE}\|$ = 10V, t_{ON} = 10ms, V_O = 0V	4	3	Apk (min)
V_{OD} (8)	Output Dropout Voltage (9)	$\|V_{CC}–V_O\|$, V_{CC} = 20V, I_O = +100mA	1.5	4	V (max)
		$\|V_O–V_{EE}\|$, V_{EE} = −20V, I_O = −100mA	2.5	4	V (max)
PSRR (8)	Power Supply Rejection Ratio	V_{CC} = 30V to 10V, V_{EE} = −30V, V_{CM} = 0V, I_O = 0mA	125	85	dB (min)
		V_{CC} = 30V, V_{EE} = −30V to −10V V_{CM} = 0V, I_O = 0mA	110	85	dB (min)
CMRR (8)	Common Mode Rejection Ratio	V_{CC} = 50V to 10V, V_{EE} = −10V to −50V, V_{CM} = 20V to −20V, I_O = 0mA	110	75	dB (min)
A_{VOL} (8)	Open Loop Voltage Gain	R_L = 2kΩ, ΔV_O = 40V	115	80	dB (min)
GBWP	Gain Bandwidth Product	f_O = 100kHz, V_{IN} = 50mVrms	8	2	MHz (min)
e_{IN} (6)	Input Noise	IHF–A Weighting Filter, R_{IN} = 600Ω (Input Referred)	2.0	8	μV (max)
SNR	Signal-to-Noise Ratio	P_O = 1W, A–Weighted, Measured at 1kHz, R_S = 25Ω	98		dB
		P_O = 25W, A–Weighted Measured at 1kHz, R_S = 25Ω	112		dB
A_M	Mute Attenuation	Pin 6,11 at 2.5V	115	80	dB (min)

(1) All voltages are measured with respect to the GND pins (5, 10), unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specifications that all parts are tested in production to meet the stated values.
(5) V_{EE} must have at least −9V at its pin with reference to ground in order for the under-voltage protection circuitry to be disabled. In addition, the voltage differential between V_{CC} and V_{EE} must be greater than 14V.
(6) AC Electrical Test; Refer to Test Circuit #2 .
(7) When using the isolated package (NDB), the θ_{JC} is 2°C/W verses 1°C/W for the non-isolated package (NDL). This increased thermal resistance from junction to case requires a lower supply voltage for decreased power dissipation within the package. Voltages higher than ±26V maybe used but will require a heat sink with less than 1°C/W thermal resistance to avoid activating thermal shutdown during normal operation.
(8) DC Electrical Test; Refer to Test Circuit #1 .
(9) The output dropout voltage, V_{OD}, is the supply voltage minus the clipping voltage. Refer to the Clipping Voltage vs. Supply Voltage graph in the TYPICAL PERFORMANCE CHARACTERISTICS section.

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Test Circuit #1

(DC Electrical Test Circuit)

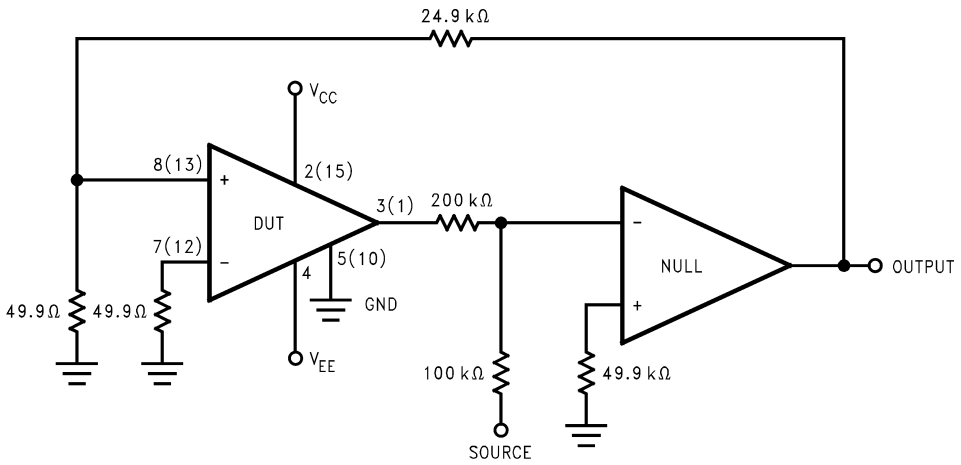


Figure 3.

Test Circuit #2

(AC Electrical Test Circuit)

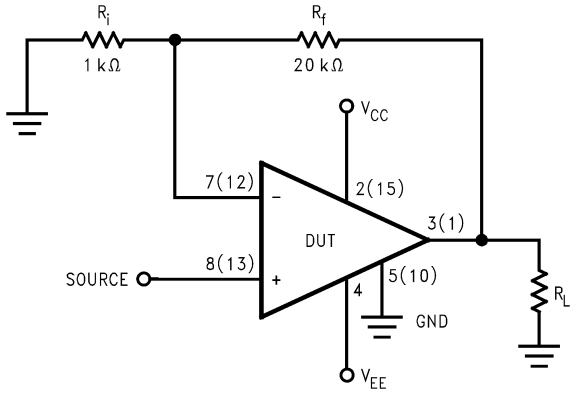


Figure 4.

BRIDGED AMPLIFIER APPLICATION CIRCUIT

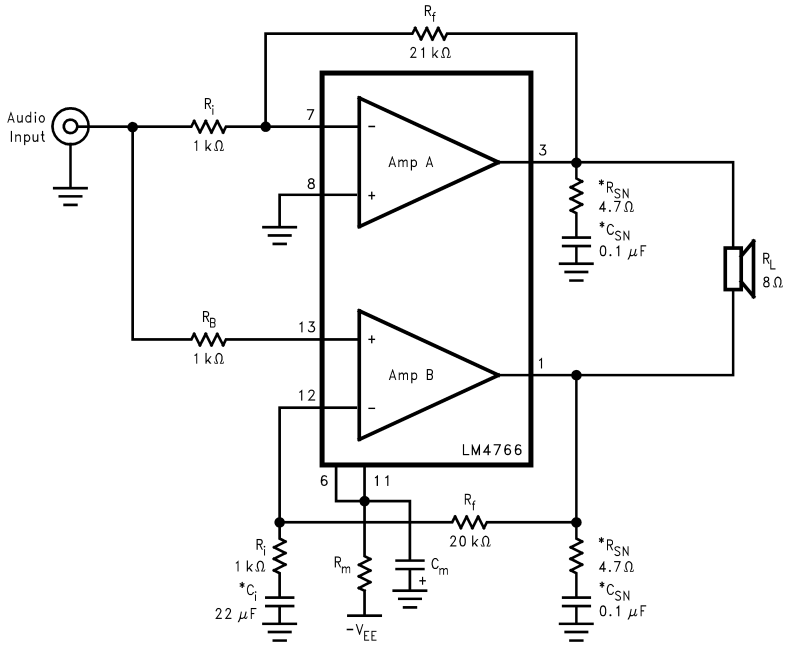
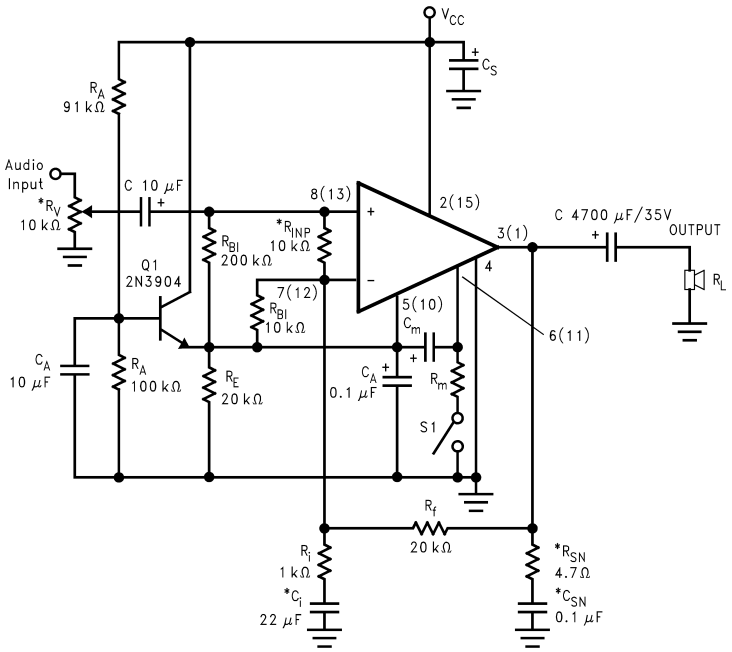


Figure 5. Bridged Amplifier Application Circuit

Single Supply Application Circuit



*Optional components dependent upon specific design requirements.

Figure 6. Single Supply Amplifier Application Circuit

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Auxiliary Amplifier Application Circuit

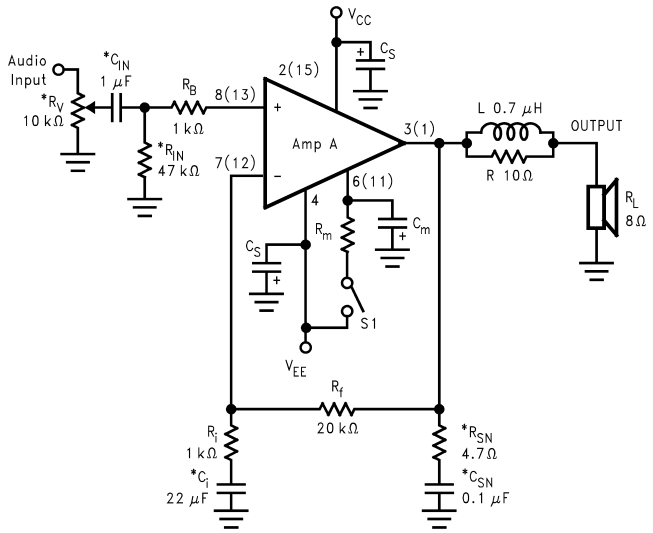
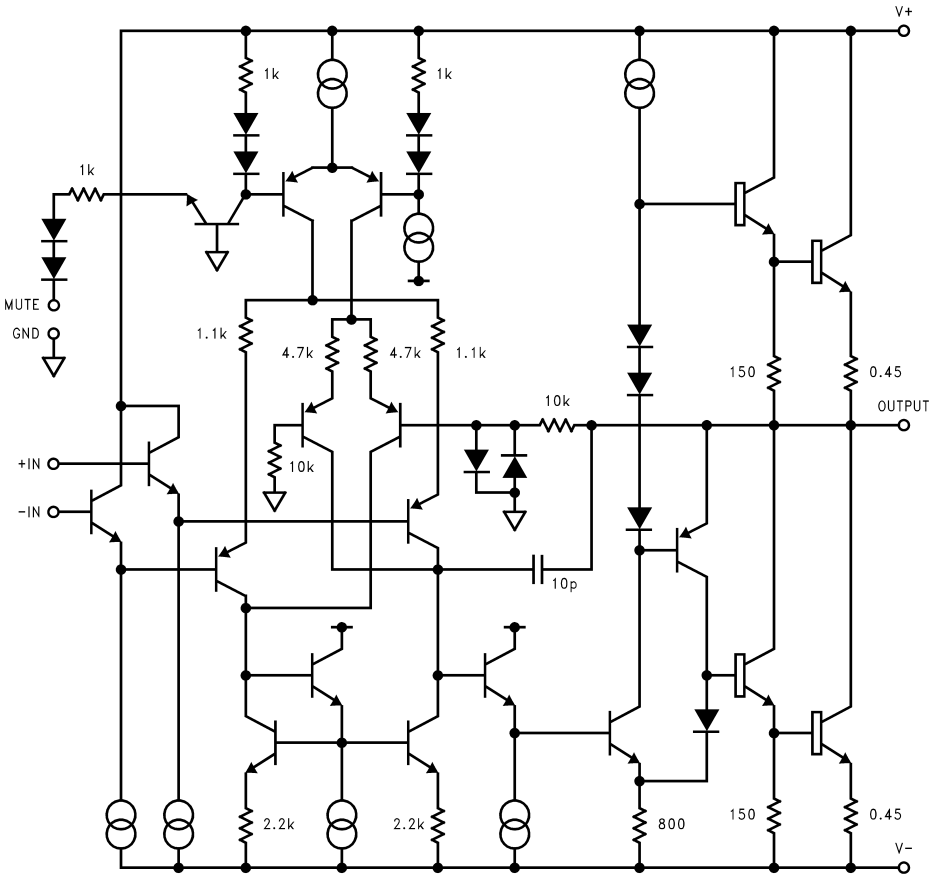


Figure 7. Special Audio Amplifier Application Circuit

Equivalent Schematic

(excluding active protection circuitry)

Figure 8. LM4766 (One Channel Only)



External Components Description

Components		Functional Description
1	R_B	Prevents currents from entering the amplifier's non-inverting input which may be passed through to the load upon power down of the system due to the low input impedance of the circuitry when the undervoltage circuitry is off. This phenomenon occurs when the supply voltages are below 1.5V.
2	R_i	Inverting input resistance to provide AC gain in conjunction with R_f.
3	R_f	Feedback resistance to provide AC gain in conjunction with R_i.
4	C_i (1)	Feedback capacitor which ensures unity gain at DC. Also creates a highpass filter with R_i at $f_C = 1/(2\pi R_i C_i)$.
5	C_S	Provides power supply filtering and bypassing. Refer to the SUPPLY BYPASSING section for proper placement and selection of bypass capacitors.
6	R_V (1)	Acts as a volume control by setting the input voltage level.
7	R_{IN} (1)	Sets the amplifier's input terminals DC bias point when C_{IN} is present in the circuit. Also works with C_{IN} to create a highpass filter at $f_C = 1/(2\pi R_{IN} C_{IN})$. Refer to Figure 7.
8	C_{IN} (1)	Input capacitor which blocks the input signal's DC offsets from being passed onto the amplifier's inputs.
9	R_{SN} (1)	Works with C_{SN} to stabilize the output stage by creating a pole that reduces high frequency instabilities.
10	C_{SN} (1)	Works with R_{SN} to stabilize the output stage by creating a pole that reduces high frequency instabilities. The pole is set at $f_C = 1/(2\pi R_{SN} C_{SN})$. Refer to Figure 7.
11	L (1)	Provides high impedance at high frequencies so that R may decouple a highly capacitive load and reduce the Q of the series resonant circuit. Also provides a low impedance at low frequencies to short out R and pass audio signals to the load. Refer to Figure 7.
12	R (1)	
13	R_A	Provides DC voltage biasing for the transistor Q1 in single supply operation.
14	C_A	Provides bias filtering for single supply operation.
15	R_{INP} (1)	Limits the voltage difference between the amplifier's inputs for single supply operation. Refer to the CLICKS AND POPS application section for a more detailed explanation of the function of R_{INP}.
16	R_{BI}	Provides input bias current for single supply operation. Refer to the CLICKS AND POPS application section for a more detailed explanation of the function of R_{BI}.
17	R_E	Establishes a fixed DC current for the transistor Q1 in single supply operation. This resistor stabilizes the half-supply point along with C_A.
18	R_M	Mute resistance set up to allow 0.5mA to be drawn from pin 6 or 11 to turn the muting function off. → R_M is calculated using: $R_M \leq (\lvert V_{EE} \rvert - 2.6V)/I$ where $I \geq 0.5mA$. Refer to the Mute Attenuation vs Mute Current curves in the TYPICAL PERFORMANCE CHARACTERISTICS section.
19	C_M	Mute capacitance set up to create a large time constant for turn-on and turn-off muting.
20	S_1	Mute switch that mutes the music going into the amplifier when opened.

(1) Optional components dependent upon specific design requirements.

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TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Frequency

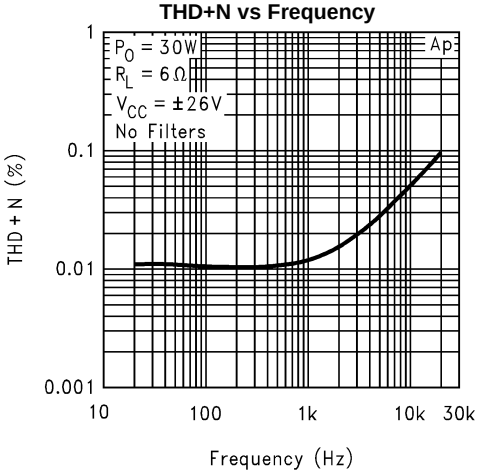

Figure 9.

THD+N vs Frequency

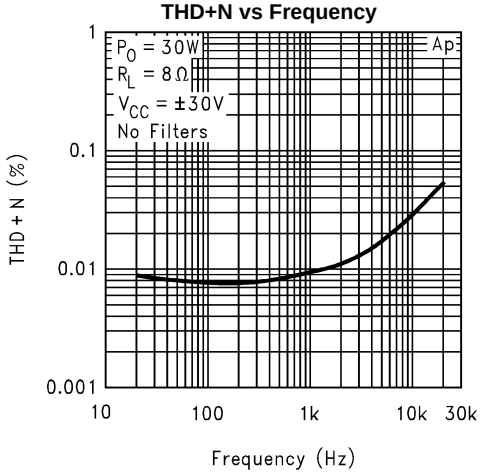

Figure 10.

THD+N vs Output Power

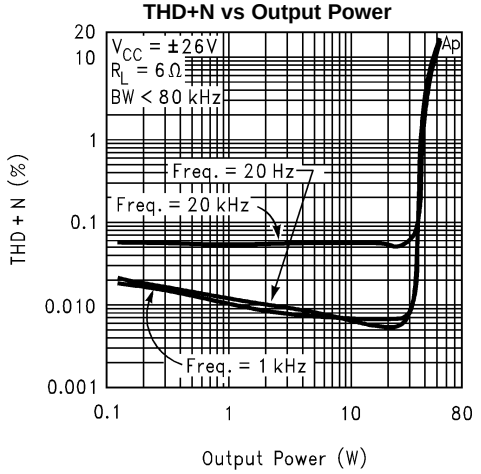

Figure 11.

THD+N vs Output Power

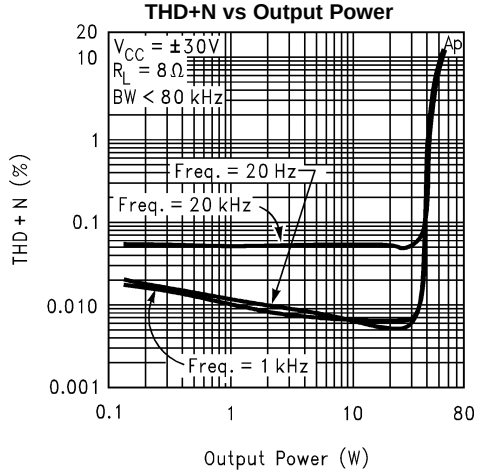

Figure 12.

THD+N vs Distribution

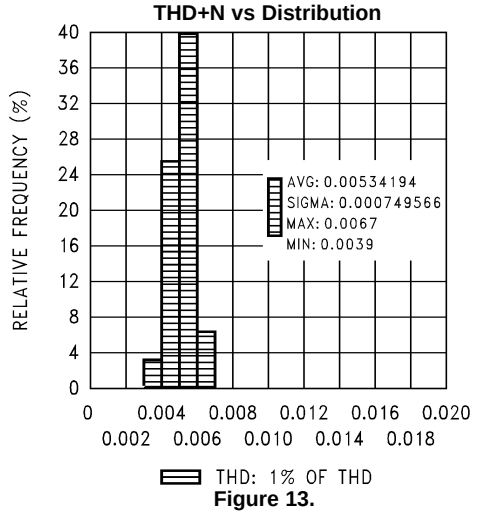

Figure 13.

THD+N vs Distribution

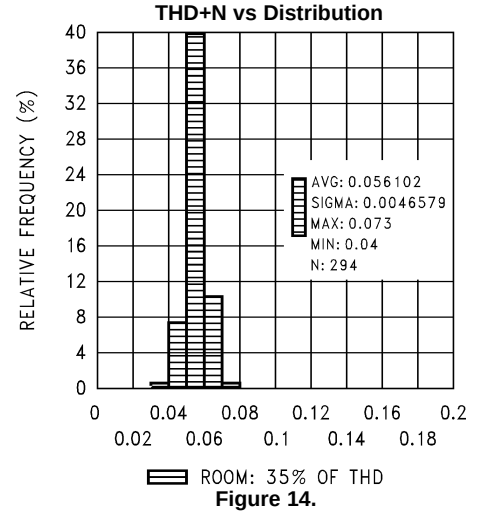

Figure 14.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Channel Separation vs Frequency

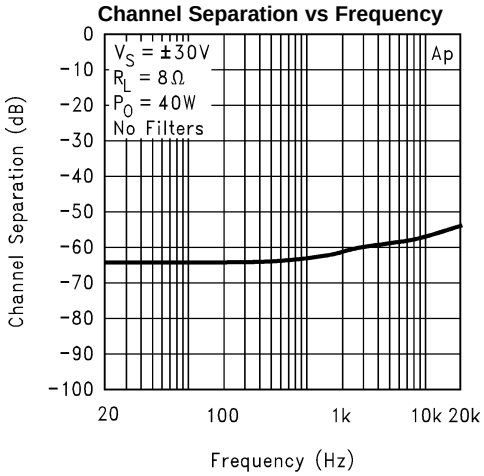

Figure 15.

Clipping Voltage vs Supply Voltage

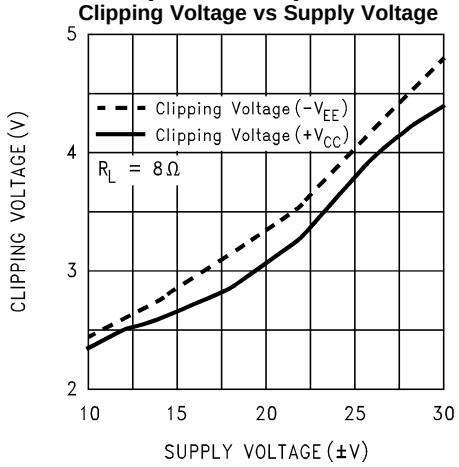

Figure 16.

Output Power vs Load Resistance

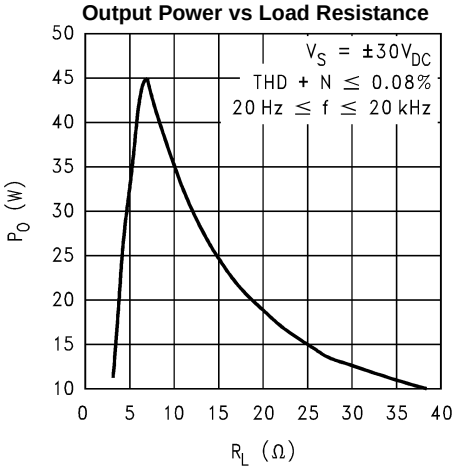

Figure 17.

Output Power vs Supply Voltage

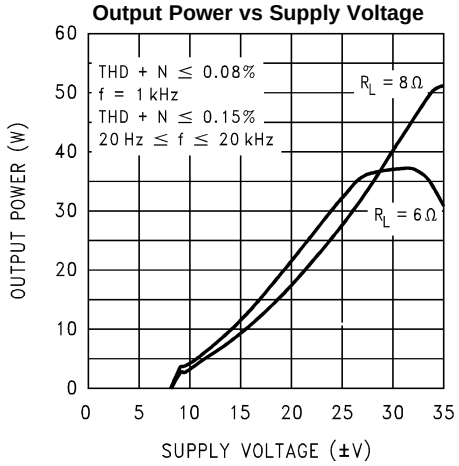

Figure 18.

Power Dissipation vs Output Power

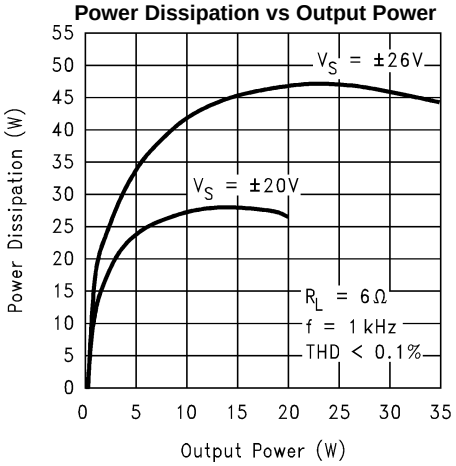

Figure 19.

Power Dissipation vs Output Power

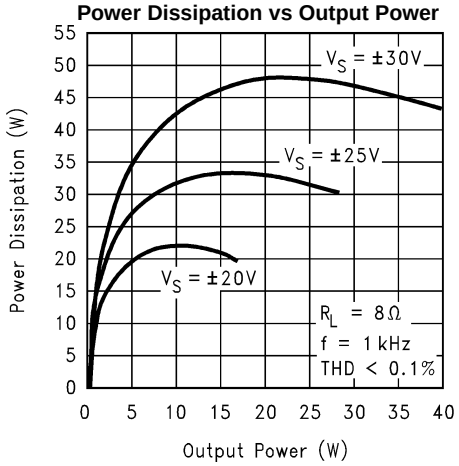

Figure 20.

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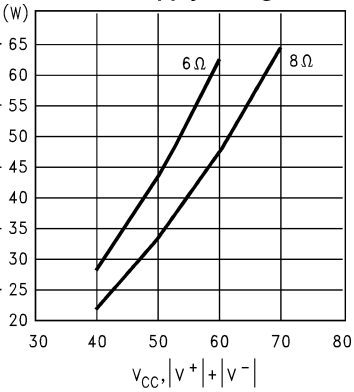
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Max Heatsink Thermal Resistance (°C/W) at the Specified Ambient Temperature (°C)

T_A = 25°C	40	50	60	70	80	90	100	P_D (W)
0.72								65
0.88								60
1.07	0.80							55
1.30	1.00	0.80						50
1.58	1.24	1.02	0.80					45
1.93	1.55	1.30	1.05	0.80				40
2.37	1.94	1.66	1.37	1.09	0.80			35
2.97	2.47	2.13	1.80	1.47	1.13	0.80		30
3.80	3.20	2.80	2.40	2.00	1.60	1.20	0.80	25
5.05	4.30	3.80	3.30	2.80	2.30	1.80	1.30	20

Maximum Power Dissipation vs. Supply Voltage



Note: The maximum heatsink thermal resistance values, θ_{SA}, in the table above were calculated using a θ_{CS} = 0.2°C/W due to thermal compound.

Figure 21.

Safe Area

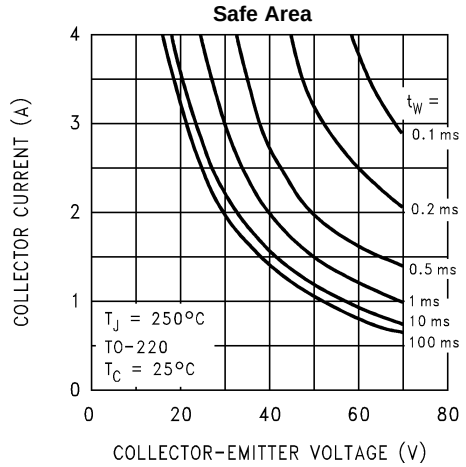


Figure 22.

SPiKe Protection Response

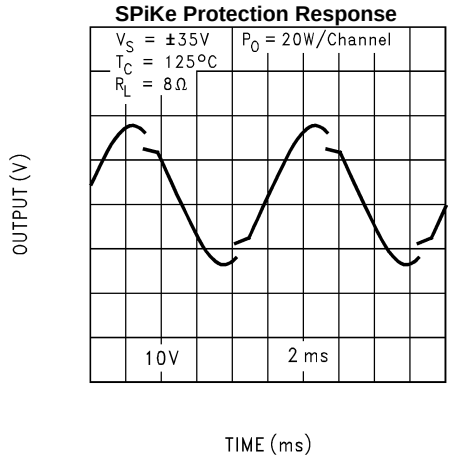


Figure 23.

Pulse Power Limit

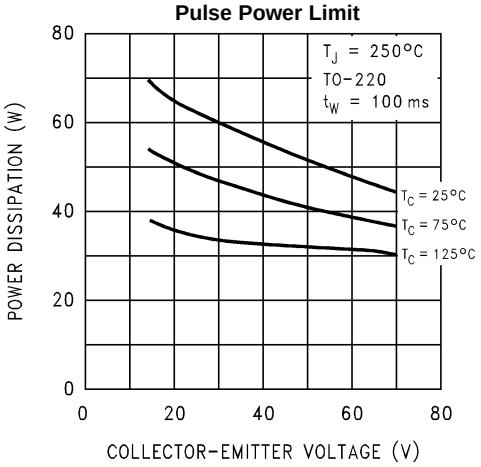


Figure 24.

Pulse Power Limit

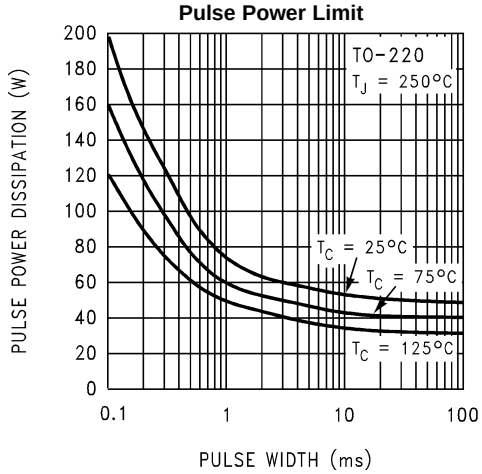


Figure 25.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Pulse Response

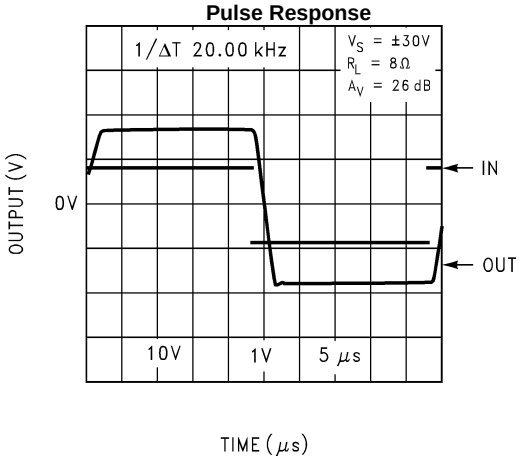


Figure 26.

Large Signal Response

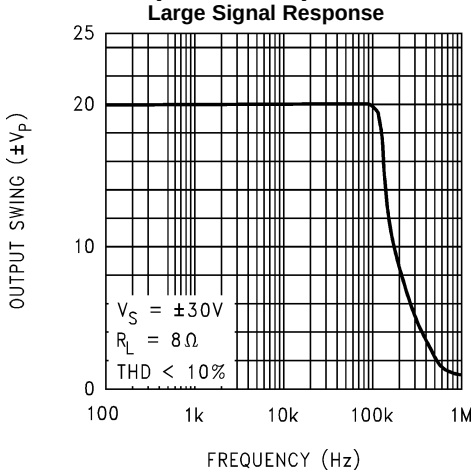


Figure 27.

Power Supply Rejection Ratio

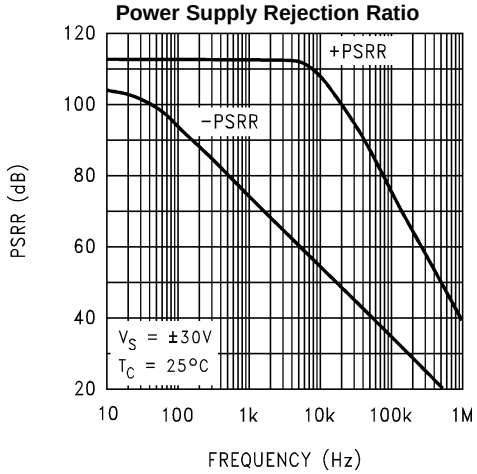


Figure 28.

Common-Mode Rejection Ratio

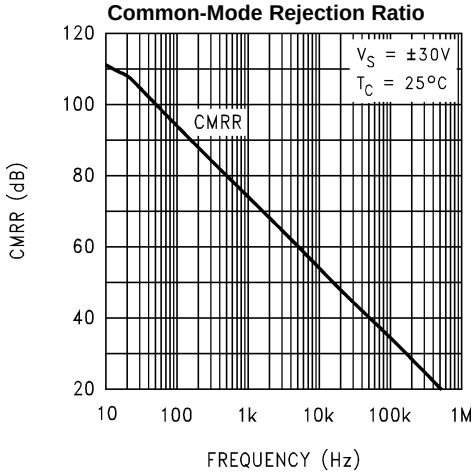


Figure 29.

Open Loop Frequency Response

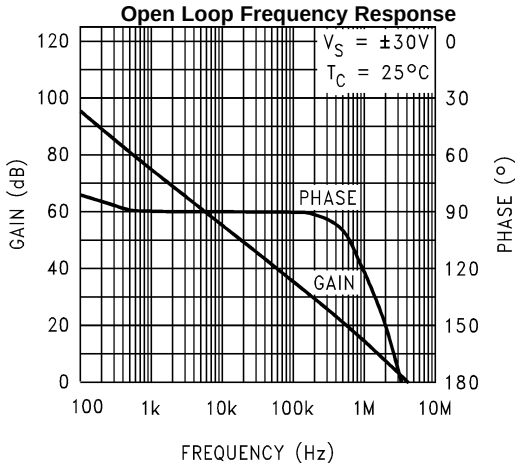


Figure 30.

Supply Current vs Case Temperature

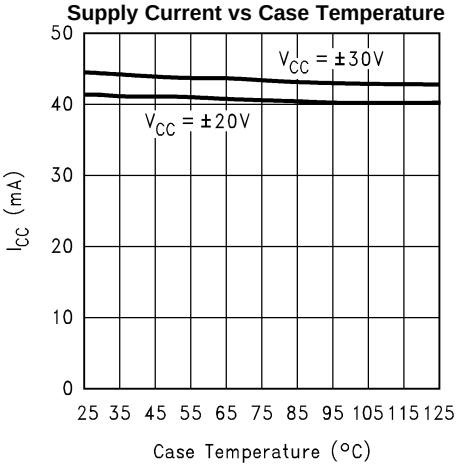


Figure 31.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Input Bias Current vs Case Temperature

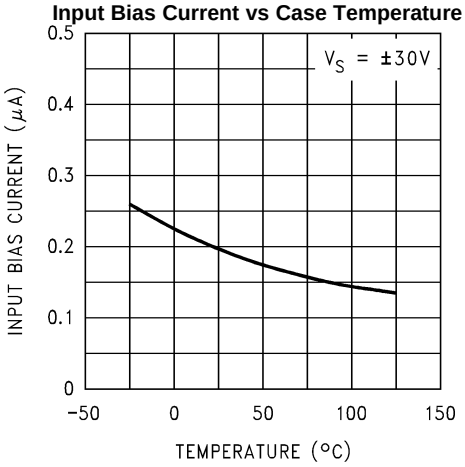

Figure 32.

Mute Attenuation vs Mute Current (per Amplifier)

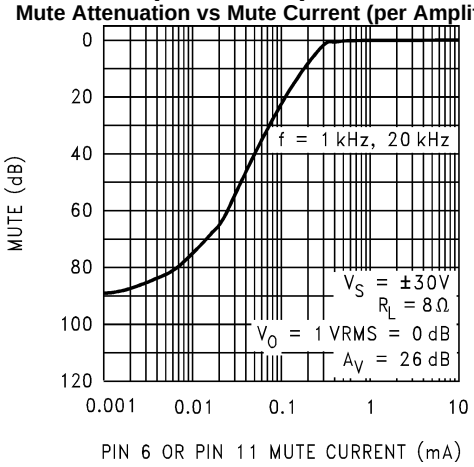

Figure 33.

Mute Attenuation vs Mute Current (per Amplifier)

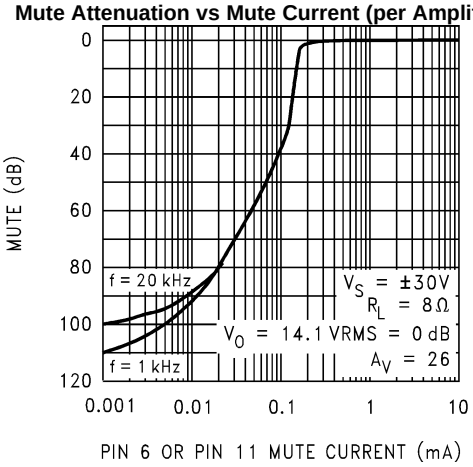

Figure 34.

Output Power/Channel vs Supply Voltage
f = 1kHz, R_L = 4Ω, 80kHz BW

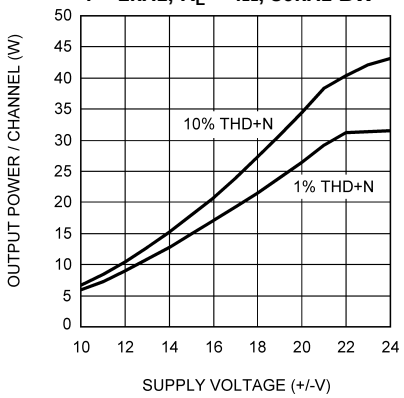

Figure 35.

Output Power/Channel vs Supply Voltage
f = 1kHz, R_L = 6Ω, 80kHz BW

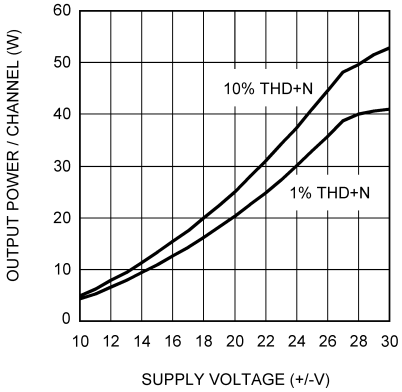

Figure 36.

Output Power/Channel vs Supply Voltage
f = 1kHz, R_L = 8Ω, 80kHz BW

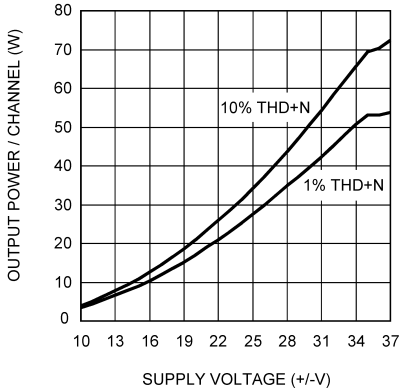

Figure 37.

APPLICATION INFORMATION

MUTE MODE

The muting function of the LM4766 allows the user to mute the music going into the amplifier by drawing more than 0.5mA out of each mute pin on the device. This is accomplished as shown in the Typical Application Circuit where the resistor R_M is chosen with reference to your negative supply voltage and is used in conjunction with a switch. The switch when opened cuts off the current flow from pin 6 or 11 to $-V_{EE}$, thus placing the LM4766 into mute mode. Refer to the Mute Attenuation vs Mute Current curves in the TYPICAL PERFORMANCE CHARACTERISTICS section for values of attenuation per current out of pins 6 or 11. The resistance R_M is calculated by the following equation:

$R_M \leq (|-V_{EE}| - 2.6V)/I_{pin6}$

where

- $I_{pin6} = I_{pin11} \geq 0.5mA.$ (1)

Both pins 6 and 11 can be tied together so that only one resistor and capacitor are required for the mute function. The mute resistance must be chosen such that greater than 1mA is pulled through the resistor R_M so that each amplifier is fully pulled out of mute mode. Taking into account supply line fluctuations, it is a good idea to pull out 1mA per mute pin or 2 mA total if both pins are tied together.

UNDER-VOLTAGE PROTECTION

Upon system power-up, the under-voltage protection circuitry allows the power supplies and their corresponding capacitors to come up close to their full values before turning on the LM4766 such that no DC output spikes occur. Upon turn-off, the output of the LM4766 is brought to ground before the power supplies such that no transients occur at power-down.

OVER-VOLTAGE PROTECTION

The LM4766 contains over-voltage protection circuitry that limits the output current to approximately $4.0A_{PK}$ while also providing voltage clamping, though not through internal clamping diodes. The clamping effect is quite the same, however, the output transistors are designed to work alternately by sinking large current spikes.

SPiKe PROTECTION

The LM4766 is protected from instantaneous peak-temperature stressing of the power transistor array. The Safe Operating graph in the TYPICAL PERFORMANCE CHARACTERISTICS section shows the area of device operation where **SPiKe** Protection Circuitry is not enabled. The waveform to the right of the SOA graph exemplifies how the dynamic protection will cause waveform distortion when enabled. Please refer to AN-898 for more detailed information.

THERMAL PROTECTION

The LM4766 has a sophisticated thermal protection scheme to prevent long-term thermal stress of the device. When the temperature on the die reaches 165°C, the LM4766 shuts down. It starts operating again when the die temperature drops to about 155°C, but if the temperature again begins to rise, shutdown will occur again at 165°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will cause the device to cycle in a Schmitt Trigger fashion between the thermal shutdown temperature limits of 165°C and 155°C. This greatly reduces the stress imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink used, the heat sink should be chosen such that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device, as discussed in the DETERMINING THE CORRECT HEAT SINK section.

DETERMINING MAXIMUM POWER DISSIPATION

Power dissipation within the integrated circuit package is a very important parameter requiring a thorough understanding if optimum power output is to be obtained. An incorrect maximum power dissipation calculation may result in inadequate heat sinking causing thermal shutdown and thus limiting the output power.

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Equation 2 exemplifies the theoretical maximum power dissipation point of each amplifier where V_{CC} is the total supply voltage.

$$P_{DMAX} = V_{CC}^2/2\pi^2R_L \quad (2)$$

Thus by knowing the total supply voltage and rated output load, the maximum power dissipation point can be calculated. The package dissipation is twice the number which results from Equation 2 since there are two amplifiers in each LM4766. Refer to the graphs of Power Dissipation versus Output Power in the TYPICAL PERFORMANCE CHARACTERISTICS section which show the actual full range of power dissipation not just the maximum theoretical point that results from Equation 2.

DETERMINING THE CORRECT HEAT SINK

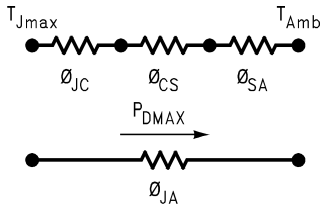
The choice of a heat sink for a high-power audio amplifier is made entirely to keep the die temperature at a level such that the thermal protection circuitry does not operate under normal circumstances.

The thermal resistance from the die (junction) to the outside air (ambient) is a combination of three thermal resistances, θ_{JC}, θ_{CS}, and θ_{SA}. In addition, the thermal resistance, θ_{JC} (junction to case), of the LM4766T is 1°C/W. Using Thermalloy Thermacote thermal compound, the thermal resistance, θ_{CS} (case to sink), is about 0.2°C/W. Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LM4766 is equal to the following:

$$P_{DMAX} = (T_{JMAX} - T_{AMB})/\theta_{JA}$$

where

- T_{JMAX} = 150°C, T_{AMB} is the system ambient temperature
- $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ (3)



Once the maximum package power dissipation has been calculated using Equation 2, the maximum thermal resistance, θ_{SA}, (heat sink to ambient) in °C/W for a heat sink can be calculated. This calculation is made using Equation 4 which is derived by solving for θ_{SA} in Equation 3.

$$\theta_{SA} = [(T_{JMAX} - T_{AMB}) - P_{DMAX}(\theta_{JC} + \theta_{CS})]/P_{DMAX} \quad (4)$$

Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier requirements. If the ambient temperature that the audio amplifier is to be working under is higher than 25°C, then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller.

SUPPLY BYPASSING

The LM4766 has excellent power supply rejection and does not require a regulated supply. However, to improve system performance as well as eliminate possible oscillations, the LM4766 should have its supply leads bypassed with low-inductance capacitors having short leads that are located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as “motorboating” or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large tantalum or electrolytic capacitor (10µF or larger) which is used to absorb low frequency variations and a small ceramic capacitor (0.1µF) to prevent any high frequency feedback through the power supply lines.

If adequate bypassing is not provided, the current in the supply leads which is a rectified component of the load current may be fed back into internal circuitry. This signal causes distortion at high frequencies requiring that the supplies be bypassed at the package terminals with an electrolytic capacitor of 470µF or more.

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BRIDGED AMPLIFIER APPLICATION

The LM4766 has two operational amplifiers internally, allowing for a few different amplifier configurations. One of these configurations is referred to as “bridged mode” and involves driving the load differentially through the LM4766's outputs. This configuration is shown in Figure 5. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of its load is connected to ground.

A bridge amplifier design has a distinct advantage over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Consequently, theoretically four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped.

A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. For each operational amplifier in a bridge configuration, the internal power dissipation will increase by a factor of two over the single ended dissipation. Thus, for an audio power amplifier such as the LM4766, which has two operational amplifiers in one package, the package dissipation will increase by a factor of four. To calculate the LM4766's maximum power dissipation point for a bridged load, multiply Equation 2 by a factor of four.

This value of P_{DMAX} can be used to calculate the correct size heat sink for a bridged amplifier application. Since the internal dissipation for a given power supply and load is increased by using bridged-mode, the heatsink's θ_{SA} will have to decrease accordingly as shown by Equation 4. Refer to the section, DETERMINING THE CORRECT HEAT SINK for a more detailed discussion of proper heat sinking for a given application.

SINGLE-SUPPLY AMPLIFIER APPLICATION

The typical application of the LM4766 is a split supply amplifier. But as shown in Figure 6, the LM4766 can also be used in a single power supply configuration. This involves using some external components to create a half-supply bias which is used as the reference for the inputs and outputs. Thus, the signal will swing around half-supply much like it swings around ground in a split-supply application. Along with proper circuit biasing, a few other considerations must be accounted for to take advantage of all of the LM4766 functions, like the mute function.

CLICKS AND POPS

In the typical application of the LM4766 as a split-supply audio power amplifier, the IC exhibits excellent “click” and “pop” performance when utilizing the mute mode. In addition, the device employs Under-Voltage Protection, which eliminates unwanted power-up and power-down transients. The basis for these functions are a stable and constant half-supply potential. In a split-supply application, ground is the stable half-supply potential. But in a single-supply application, the half-supply needs to charge up just like the supply rail, V_{CC}. This makes the task of attaining a clickless and popless turn-on more challenging. Any uneven charging of the amplifier inputs will result in output clicks and pops due to the differential input topology of the LM4766.

To achieve a transient free power-up and power-down, the voltage seen at the input terminals should be ideally the same. Such a signal will be common-mode in nature, and will be rejected by the LM4766. In Figure 6, the resistor R_{INP} serves to keep the inputs at the same potential by limiting the voltage difference possible between the two nodes. This should significantly reduce any type of turn-on pop, due to an uneven charging of the amplifier inputs. This charging is based on a specific application loading and thus, the system designer may need to adjust these values for optimal performance.

As shown in Figure 6, the resistors labeled R_{BI} help bias up the LM4766 off the half-supply node at the emitter of the 2N3904. But due to the input and output coupling capacitors in the circuit, along with the negative feedback, there are two different values of R_{BI}, namely 10kΩ and 200kΩ. These resistors bring up the inputs at the same rate resulting in a popless turn-on. Adjusting these resistors values slightly may reduce pops resulting from power supplies that ramp extremely quick or exhibit overshoot during system turn-on.

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AUDIO POWER AMPLIFIER DESIGN

Design a 30W/8Ω Audio Amplifier

Given:

Power Output	30Wrms
Load Impedance	8Ω
Input Level	1Vrms(max)
Input Impedance	47kΩ
Bandwidth	20Hz−20kHz ±0.25dB

A designer must first determine the power supply requirements in terms of both voltage and current needed to obtain the specified output power. V_{OPEAK} can be determined from Equation 5 and I_{OPEAK} from Equation 6.

$$V_{OPEAK} = \sqrt{(2R_L P_O)} \tag{5}$$

$$I_{OPEAK} = \sqrt{(2P_O)/R_L} \tag{6}$$

To determine the maximum supply voltage the following conditions must be considered. Add the dropout voltage to the peak output swing V_{OPEAK}, to get the supply rail at a current of I_{OPEAK}. The regulation of the supply determines the unloaded voltage which is usually about 15% higher. The supply voltage will also rise 10% during high line conditions. Therefore the maximum supply voltage is obtained from the following equation.

$$\text{Max supplies} \approx \pm (V_{OPEAK} + V_{OD})\ (1 + \text{regulation})\ (1.1) \tag{7}$$

For 30W of output power into an 8Ω load, the required V_{OPEAK} is 21.91V. A minimum supply rail of 25.4V results from adding V_{OPEAK} and V_{OD}. With regulation, the maximum supplies are ±32V and the required I_{OPEAK} is 2.74A from Equation 6. It should be noted that for a dual 30W amplifier into an 8Ω load the I_{OPEAK} drawn from the supplies is twice $2.74A_{PK}$ or $5.48A_{PK}$. At this point it is a good idea to check the Power Output vs Supply Voltage to ensure that the required output power is obtainable from the device while maintaining low THD+N. In addition, the designer should verify that with the required power supply voltage and load impedance, that the required heatsink value θ_{SA} is feasible given system cost and size constraints. Once the heatsink issues have been addressed, the required gain can be determined from Equation 8.

$$A_V \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{ORMS}/V_{INRMS} \tag{8}$$

From Equation 8, the minimum A_V is: $A_V \geq 15.5$.

By selecting a gain of 21, and with a feedback resistor, $R_f = 20k\Omega$, the value of R_i follows from Equation 9.

$$R_i = R_f\ (A_V - 1) \tag{9}$$

Thus with $R_i = 1k\Omega$ a non-inverting gain of 21 will result. Since the desired input impedance was 47kΩ, a value of 47kΩ was selected for R_{IN}. The final design step is to address the bandwidth requirements which must be stated as a pair of −3dB frequency points. Five times away from a −3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified. This fact results in a low and high frequency pole of 4Hz and 100kHz respectively. As stated in the External Components Description section, R_i in conjunction with C_i create a high-pass filter.

$$C_i \geq 1/(2\pi * 1k\Omega * 4Hz) = 39.8\mu F; \quad \text{use } 39\mu F. \tag{10}$$

The high frequency pole is determined by the product of the desired high frequency pole, f_H, and the gain, A_V. With a $A_V = 21$ and $f_H = 100kHz$, the resulting GBWP is 2.1MHz, which is less than the ensured minimum GBWP of the LM4766 of 8MHz. This will ensure that the high frequency response of the amplifier will be no worse than 0.17dB down at 20kHz which is well within the bandwidth requirements of the design.

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REVISION HISTORY

Changes from Revision E (March 2013) to Revision #IMPLIED	Page

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4766T/LF15	ACTIVE	TO-220	NEK	15	20	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM4766T	Samples
LM4766T/NOPB	ACTIVE	TO-220	NDL	15	20	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM4766T	Samples
LM4766TF/NOPB	ACTIVE	TO-220	NDB	15	20	Pb-Free (RoHS Exempt)	CU SN	Level-1-NA-UNLIM	0 to 70	LM4766TF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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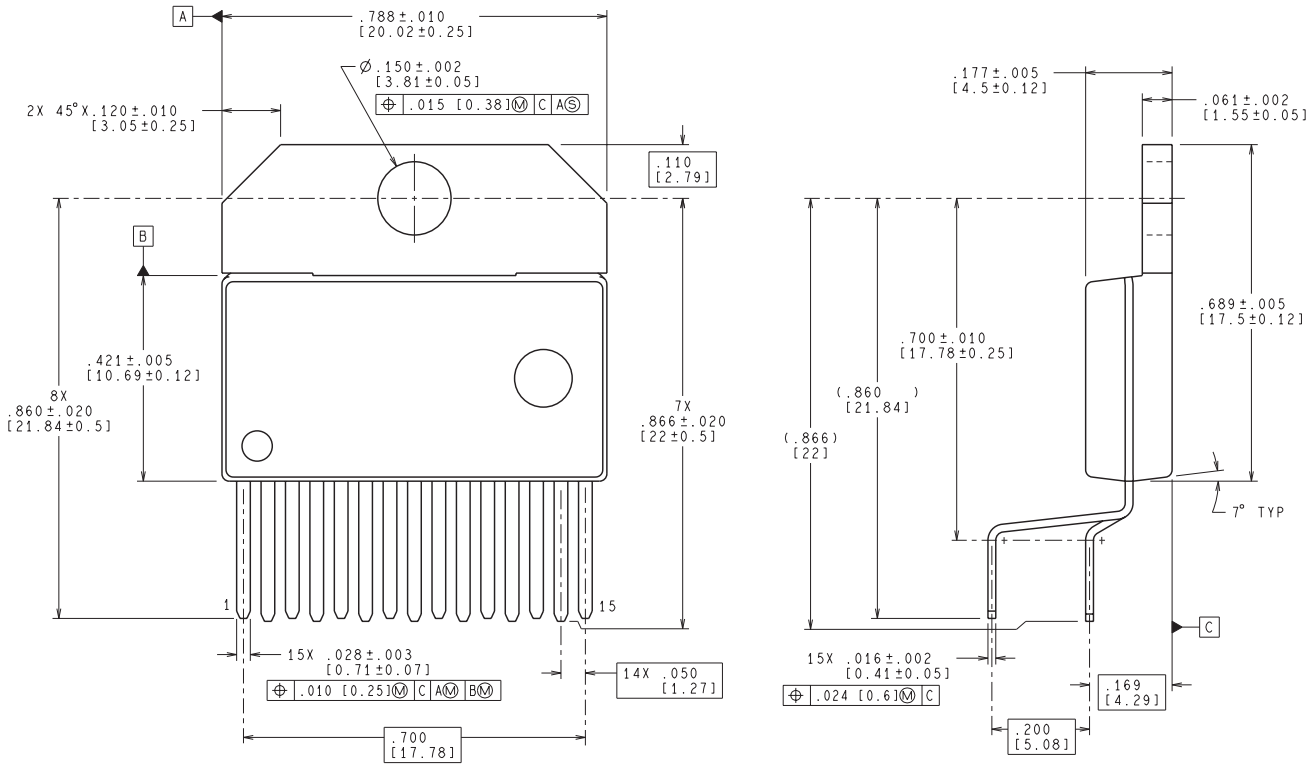

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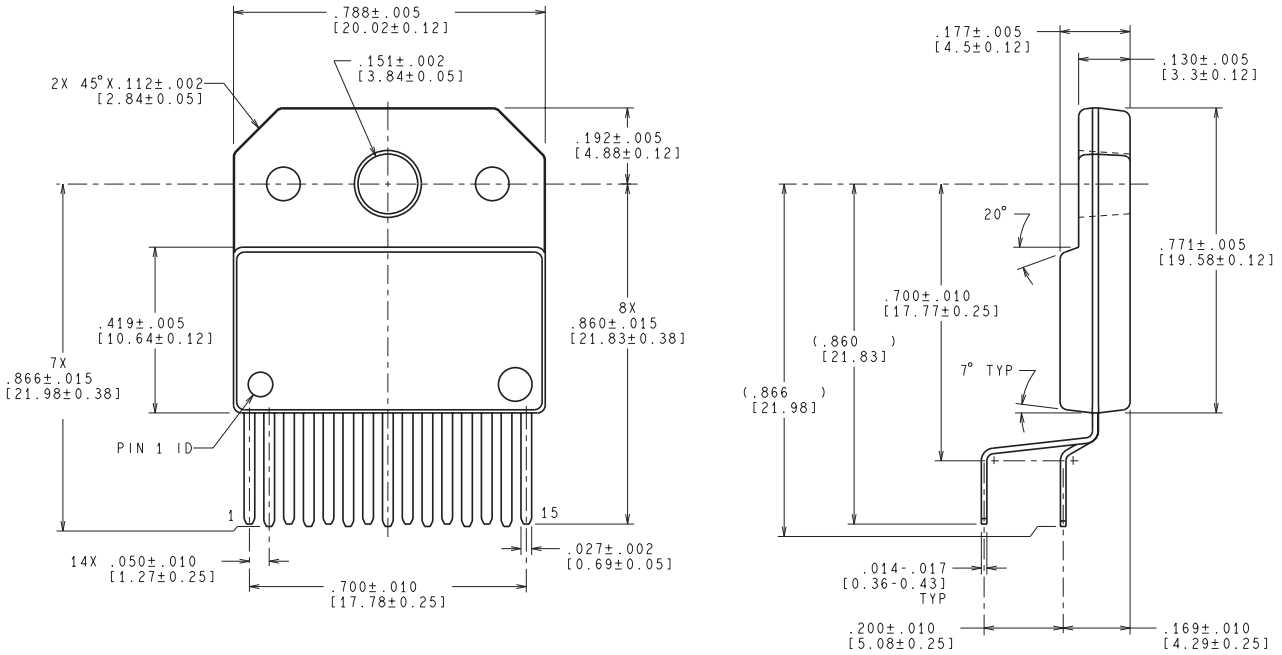

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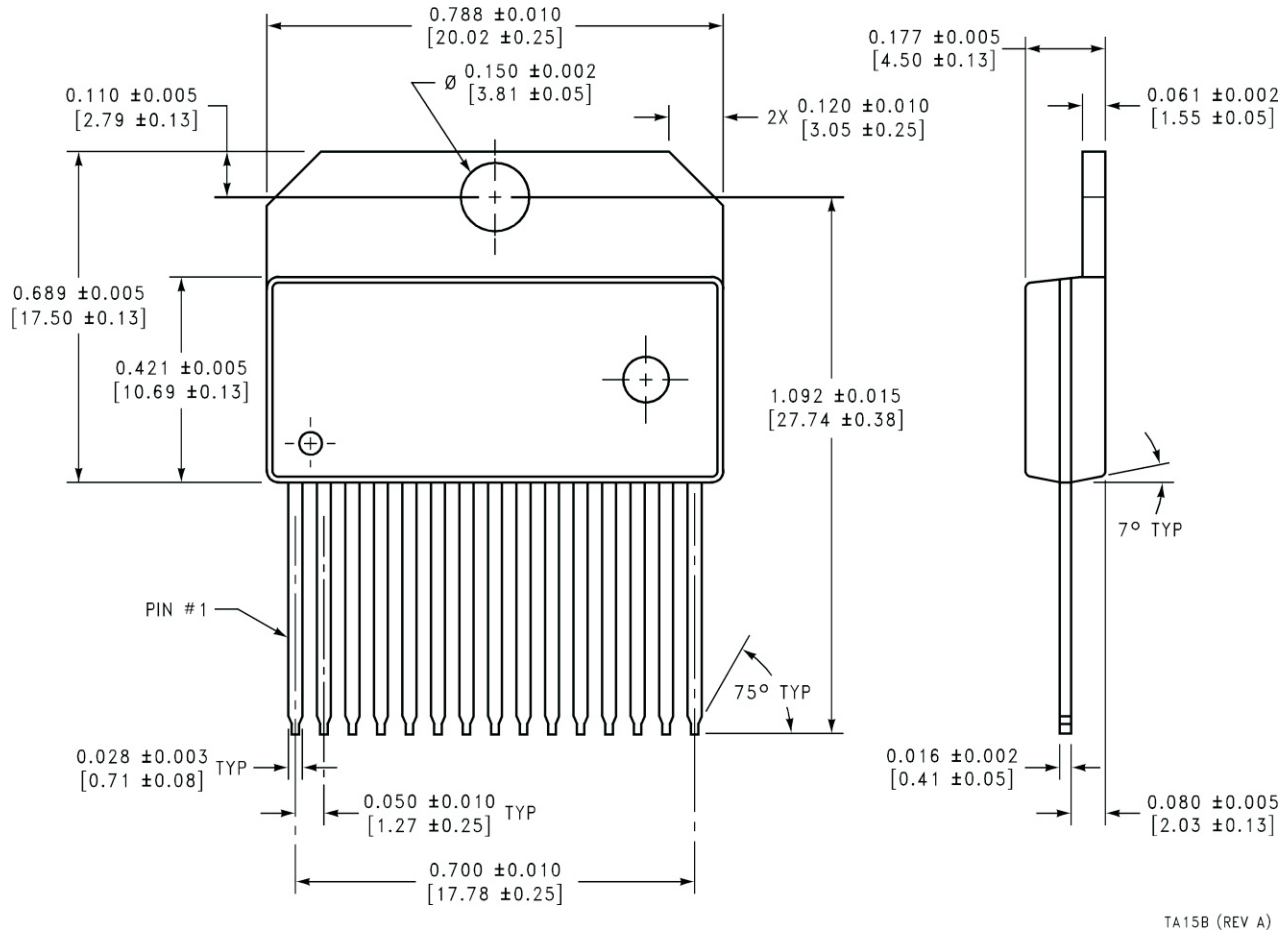
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0.700 ±0.010
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